

Lumistar LS-45-B1 Modular PCM Bit Synchronizer Quick Start Guide



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1 Introduction

1.1 General Information

This guide was created to help familiarize the user with the operations of the LS-45-B1 Modular PCM Bit Synchronizer. This manual is primarily focused on providing a quick guide to interconnections with the device and to provide a simple overview of connecting and using the provided host software application.

1.2 Specifications

The LS-45-B1 modular PCM Bit Synchronizer provides an interface for up to two PCM data streams. The module provides translation of the PCM stream(s), provides a user programmable PCM output format with correlated clock, and can even provide a combined output which represents the best of two incoming streams. The outputs generated may be recorded or provided to further processing functions. The module includes a receive BER detector for each input channel as well as an onboard frame synchronization detector. These detectors allows the checking of input data streams for test and validation functions. Data rates are user programmable in the range of 1kbps to 45Mbps (NRZ data rates).

The device can be powered by a single power input source in the range of 9VDC to 36VDC. There are up to two user interfaces to the module. The most common interface is a network 10/100Mbps Ethernet interface. An optional serial interface can be provided as either USB 2.0 or RS232.

The general specifications of the module are described in Table 1-1.

LS-45-B1 Modular PCM Synchronizer - Quick Start Guide

Specification:	Details:	Options:
Dimensions	7.75"(L) x 4.00"(W) x 1.11" (H)	
Weight	<16 oz.	
Input Power	9-36VDC; <15 Watts Max.	
Control/Status Interface	10/100Mbps Ethernet	Standard
	USB 2.0	Optional
	RS232	Optional
PCM Channels	1 or 2	
Inputs per Channel	4 Single-Ended, 2 Differential	Dual Channel option
	8 Single-Ended, 4 Differential	Single Channel Option
Single-End Imped.	50, 75, 120, 1K Ohm; SW Selected	
Differential Imped.	120 Ohm	
Channel Data Rate	1K-20Mbps (NRZ); 1K-10Mbps (non NRZ)	20Mbps Option
	1K-45Mbps (NRZ); 1K-22.5Mbps (non NRZ)	45Mbps Option
PCM Input Signal Range	0.15 to 10Vp-p; Max. 25V RMS	
Channel Input LBW	0.01 to 2%; SW Selected (rate dependent)	
Channel Acq. Range	+/- 4x the LBW setting	
Mean Acq. Time	100-250 bits	
Input PCM Conversions	NRZ-L/M/S, BIO-L/M/S, RNRZ-11/15/17/23,	
	RZ, DM-M/S, MDM-M/S, DBIO-M/S,	
	K7 Viterbi, K7 Viterbi NRZ-M	
Input PCM Conv. Inversion	SW Selected for each input code	
Output PCM Conversions	NRZ-L/M/S, BIO-L/M/S, RNRZ-11/15/17/23,	
	RZ, DM-M/S, MDM-M/S, DBIO-M/S,	
	K7 Viterbi, K7 Viterbi NRZ-M	
Outputs: Electrical	5V TTL; 50 Ohm drive capable	3.3V TTL
	RS-422 (Enhanced High-speed)	
Clock Output Phases	0, 90, 180, 270 Degrees; SW Selected	
Frame Sync Pattern Length	1 to 64 Bits	FSP Option Only
Frame Length	131, 071 Maximum Bits	FSP Option Only
Operation Temperature	-20 to 85 Degrees Celsius	
Storage Temperature	-40 to 100 Degrees Celsius	
Humidity, non-condensing	0-90% @ < 40C; 0-75% @ >40 C	

Table 1-1. General LS-45-B1 Specifications

1.3 Mechanical

The LS-45-B1 modular PCM Bit Synchronizer can be mounted in a standard PC hard drive bay using 4-40 UNC screws. Locations are provided which match that of standard hard drive mounting locations. Screws should be no longer than 3/8 inches to prevent damage to the interior components.

The unit can also be mounted from the top using 6-32 UNC screws at the four corners of the unit. Screws of 1 3/8 inches in length should provide sufficient mounting threads for securing the unit. Figure 1-1 shows a top view of the mounting holes.

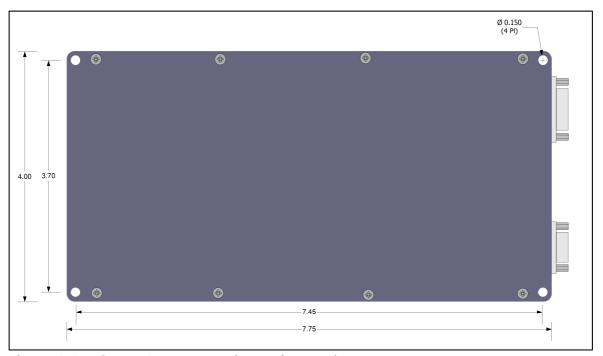


Figure 1-1. LS-45-B1 Top Mounting Hole Locations

1.4 Cabling

The LS-45-B1 modular PCM Bit Synchronizer includes four connection cables. The cables provide BNC pigtails for connecting to the unit with standard RG-Style 75 or 50 Ohm cables.

Drawings of the provided cables are shown in Figures 1-2, 1-3, 1-4, and 1-5. Connections are shown in Figure 1-6.

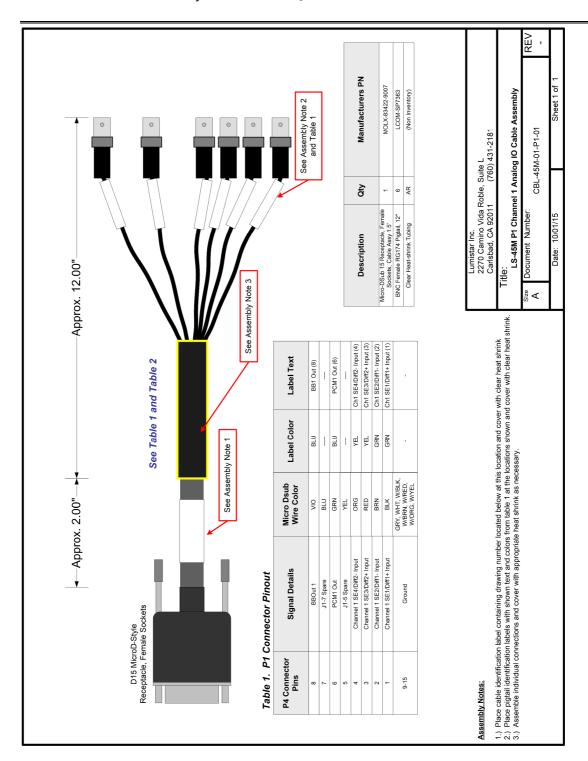


Figure 1-2. LS-45-B1 Channel 1 Analog Input/Output Cable Assembly

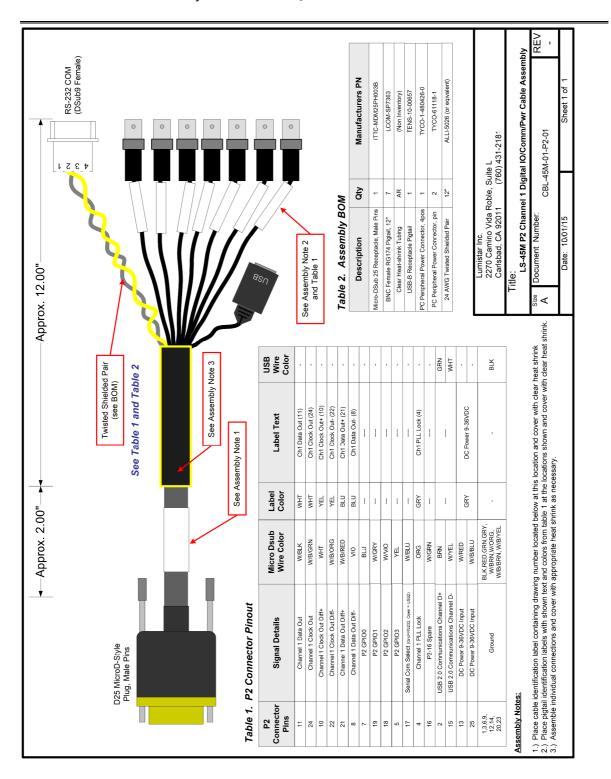


Figure 1-3. LS-45-B1 Channel 1 Digital Outputs/Comm/Power Cable Assembly

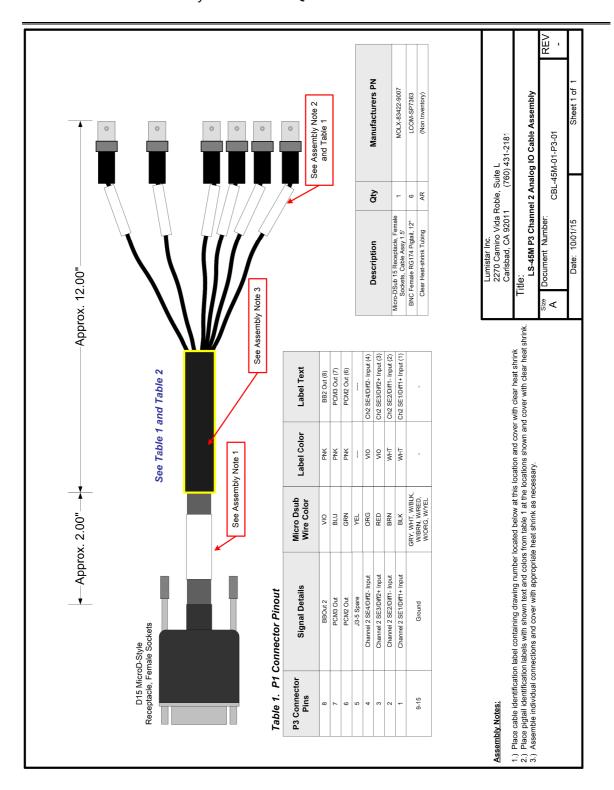


Figure 1-4. LS-45-B1 Channel 2 Analog Inputs/Outputs Cable Assembly

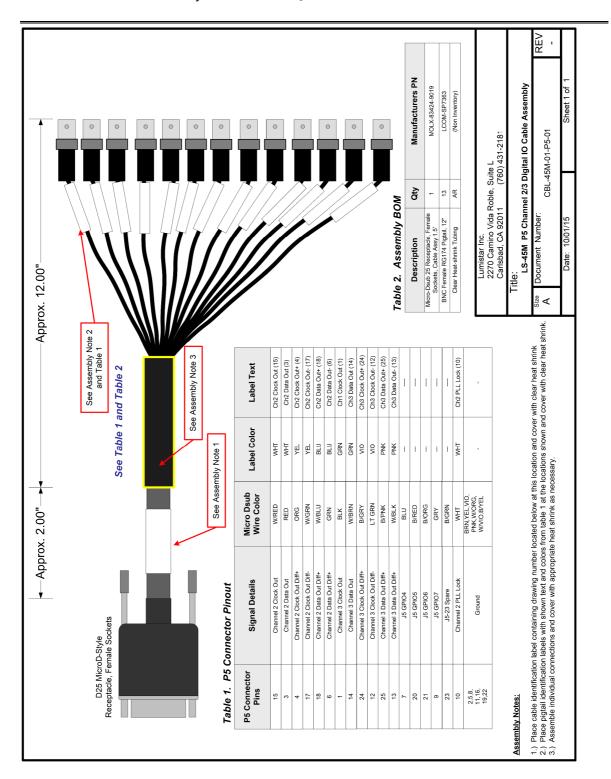


Figure 1-5. LS-45-B1 Channel 2/Combiner Digital Outputs Cable Assembly

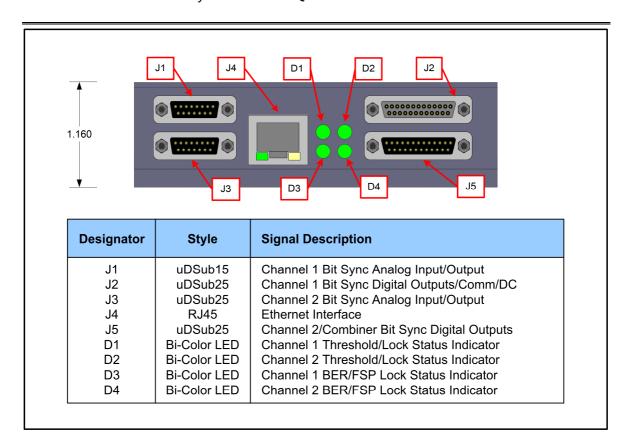


Figure 1-6. LS-45-B1 Front View - Connections

2 Control/Status Software Application

The following sections describe the initialization and use of the LS-45-B1 provided Control/Status software application. This application is a Microsoft Windows 7/8/10 (32 and 64 bit) application.

2.1 Network TCP/IP Connectivity

The TCP/IP IPv4 protocol suite requires a 5-tuple of values to establish a connection or reply to a message from a remote host.

- Transport Layer Protocol (UDP or TCP, typically).
- Local IP Address.
- Local Port Number
- Remote IP Address
- Remote Port Number

The Ethernet enabled Lumistar devices will all have an IP Address, assigned either manually or dynamically via DHCP, as well as a Port Number which will be the value of 5000. The connection will use the TCP protocol. The NetworkDevice.exe program will run on a Windows computer which will provide both the IP Address and a dynamically determined Port Number. Both the Lumistar device and the computer on which NetworkDevice.exe is running must be in the same IPv4 subnet. Ethernet enabled Lumistar devices follow the Client/Server paradigm, with the Lumistar device filling the Server role and the NetworkDevice.exe program acting as the Client.

2.2 Network Device Utilities

The LS-45-B1 product family utilizes a specific Ethernet Off-load Coprocessor. The model of this device is W7100A. The manufacturer of the interface device provides a utility for setup and control. Lumistar provides this utility with the included software. Updates to this utility may be downloaded from http://www.wiznet.co.kr.

The utility allows the user to discover configuration information of all Lumistar devices on the local subnet which use the W7100A Internet Offload Co-processor. It can also program the device with a static IP Address, or configure it to use the DHCP protocol and be dynamically assigned an IP Address. Install the WIZ107SR

Configuration Tool by executing the "setup.exe" program. After installing, select the "Config Tool" item from the "Start Menu\All Programs\WIZnet\WIZ107_108SR" menu item. Figure 2-1 shows the resulting display window.

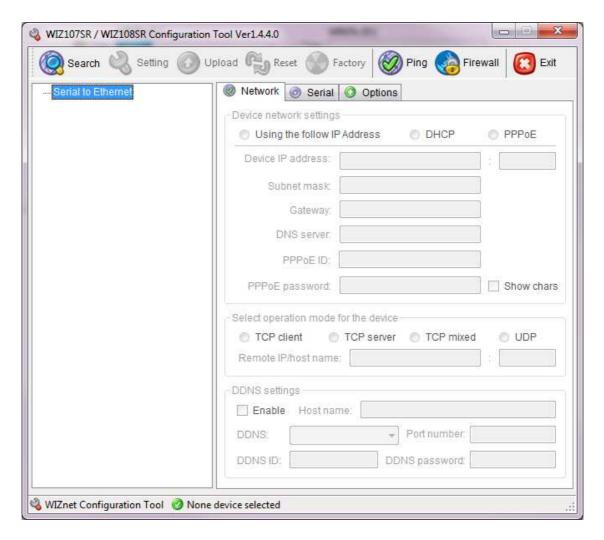


Figure 2-1. WIZ107SR Configuration Tool initialization Display Window

Press the "Search" button in the upper left hand corner. This resulting dialogue window is shown in Figure 2-2.

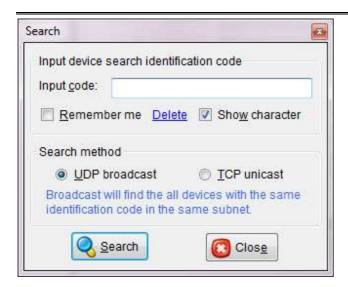


Figure 2-2. WIZ107SR Configuration Tool Search Dialogue Window

Press "Search" again, there is no need to modify any other values.

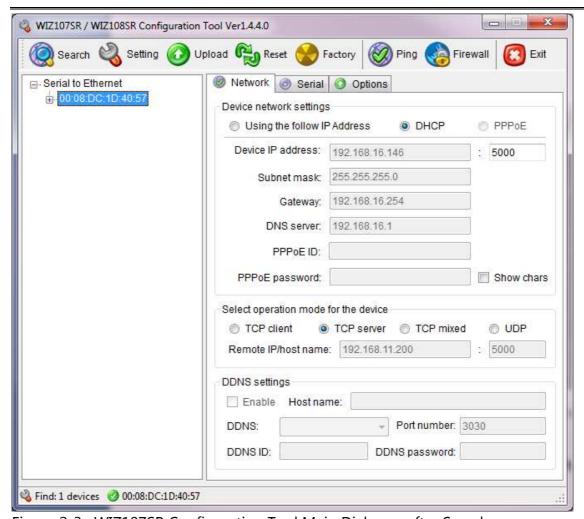


Figure 2-3. WIZ107SR Configuration Tool Main Dialogue after Search

If the search finds a Lumistar device with the W7100A chip, there will be at least one entry in left hand list tree control as shown in Figure 2-3. The items listed in this control will display the device's Ethernet MAC Address. Select the device of interest. Its configuration information will be displayed in the tab control on the right.

In general, there are two options for setting the TCP/IP network values. The user may select "Using the follow [sic] IP Address" and manually enter the IP Address and other settings. The 5000 entry represents the Port Number that the Lumistar device will listen on and must remain 5000. The second option is to select the "DHCP" radio button. On a network with a DHCP server, the Lumistar device will be able to ask the DHCP server for IP Address and other settings programmatically, without the need for manual intervention. This is the default setting that the Lumistar device will ship

from the factory in. The "PPPoE" option is not supported. In the "Select operation mode for the device" group, always select "TCP Server". "DDNS settings" should always have "Enable" unselected.

After selecting the appropriate IP Address and other settings, select the "Serial" tab as shown in Figure 2-4.

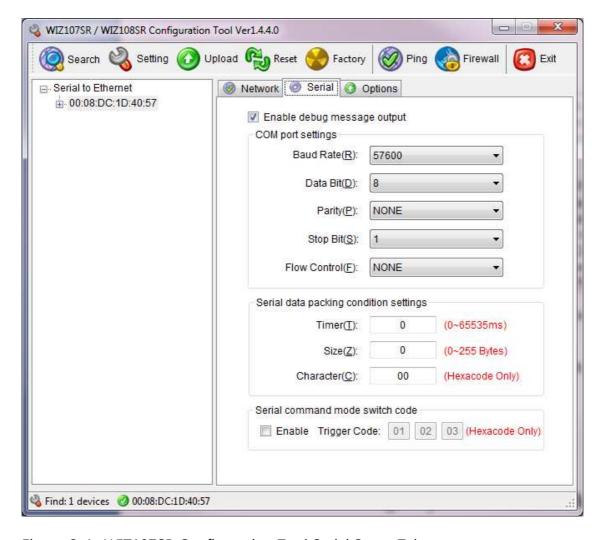


Figure 2-4. WIZ107SR Configuration Tool Serial Setup Tab.

The "COM port settings" should always be set to Baud Rate: 57600, Data Bits: 8, Parity: None, Stop Bits: 1, and Flow Control: None. All other settings should remain in their default state.

The "Options" tab settings should not be altered from their default states as shown in Figure 2-5.

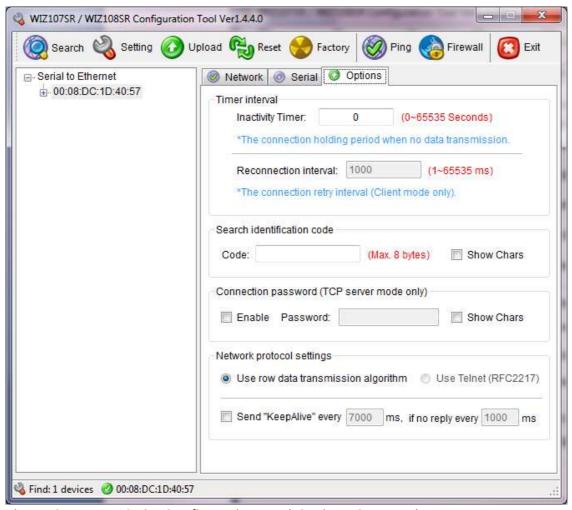


Figure 2-5. WIZ107SR Configuration Tool Options Setup Tab.

After making all selections, press the "Setting" button in the upper row next to the "Search" button. The modified settings will be saved into the Lumistar device. Power cycle the Lumistar device to allow it to restart using the new settings.

2.3 NetworkDevice.exe Control/Status Software Application

The actual LS-45-B1 Control/Status application is "generically" designated *NetworkDevice.exe*. This application is actually shared with several classes of Lumistar products.

When initially launched, the dialogue shown in Figure 2-6 will be displayed.

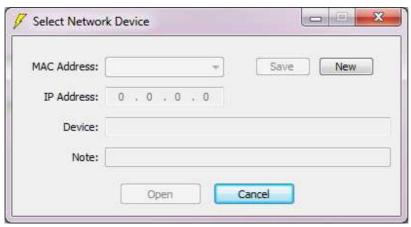


Figure 2-6. MAC Address Dialogue

NetworkDevice.exe stores configuration values. When first initiated, there are no values that have yet been saved. Press the "New" button to create the configuration values so that *NetworkDevice.exe* can open a connection to the device. See Figure 2-7.



Figure 2-7. Initial MAC Address Dialogue

Enter the MAC Address and IP Address values from the *WIZnet Config Tool* application. The Note entry is available to save user specific information in order to provide a memorable way to distinguish among more than one Lumistar devices. An example is shown in Figure 2-8.



Figure 2-8. Initial MAC Address Dialogue Example

Press the "OK" button to save the configuration information to the Windows Registry. Now the "Select Network Device" dialog should appear with configuration information in it as shown in Figure 2-9.

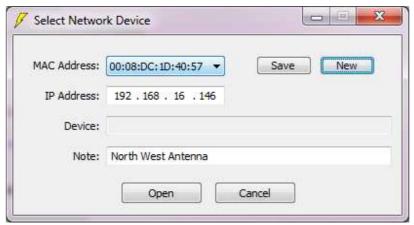


Figure 2-9. MAC Address Dialogue Example

If more than one Lumistar devices have been saved in the Registry, the user may select from among the different MAC Address values to choose a particular one. The IP Address and the Note values can be edited at this point, and saved back to the Registry by pressing the "Save" button. Press the "Open" button to open the Setup dialog of the selected Lumistar device. For the LS-45-B1, the dialogue is shown in Figure 2-10.

2.3.1 Setup BS1 and SetupBS2 Controls

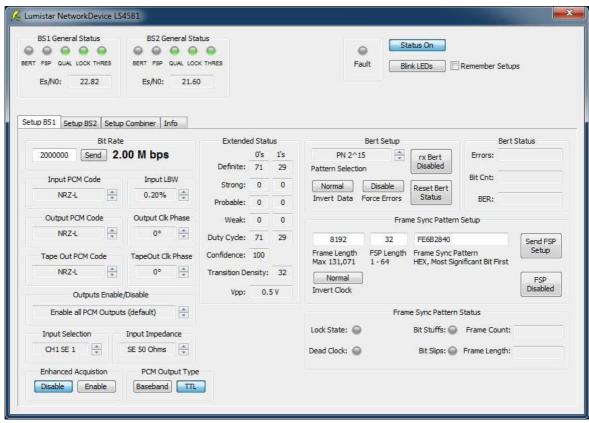


Figure 2-10. LS-45-B1 Main Dialogue

The LS-45-B1 Control/Status application contains the following controls:

Status On: This selection button provides a control for status updates. When disabled, all screen status updates are discontinued. When enabled, the status elements are updated at an approximate one second interval.

Blink LEDs: This selection button will initiate a brief flash of the control units front panel LEDs as seen in Figure 1-6. These LEDs will toggle for approximately 4 seconds alternating between green and yellow. This function is useful in identifying multiple units on a network and in verifying the communications path and physical connections. After the brief flashing of LEDs, they will resume their normal functions.

Remember Setups: This selection box, allows the setups being set in the GUI controls to be stored internally in non-volatile memory. They will be recalled and initiated between power cycles if this option is enabled.

Bit Rate: Enter the desired channel bit rate in this window. Values may be entered between 1kbps and either 20Mbps or 45Mbps, depending on the ordered configuration. Entry into the data window will not be programmed until the SEND button in this window is selected.

Send: This is primary setup control load button. Programming of all primary setup commands are initiated from this control. **This button must be commanded after all controls are set to make the settings active.**

Input PCM Code: This up/down control allows the user to select one of thirty-eight provided input PCM decoders options. This PCM decoder is applied after the incoming data bit is synchronized and correlated with an accompanying clock.

Input LBW %: This control allows the user to select one of eight loop bandwidths to be applied to the PLL acquisition and tracking synchronization loop of the PCM bit slicer. The entry is based on a percentage of the bit rate programmed and does have some correlation to data rates. These percentages vary from 0.01% to 2% of the programmed bit rate.

Output PCM Code: Similar to the Input PCM code selection, this control allows the user to select one of thirty-eight output PCM encoder methods that will be applied to the primary data output. Based on the code selections made with this control, some changes to the correlated output clock may also occur.

Output Clock Phase: The primary output clock phase can be varied in relationship to the primary data output. The clock phase can be advanced from being aligned with the rising data edge to 90, 180 and 270 degrees.

Tape Output PCM Code: This control allows the user to select one of thirty-eight output PCM encoder methods that will be applied to the tape PCM data output.

Tape Output Clock Phase: The tape output clock phase can be varied in relationship to the tape PCM data output. The clock phase can be advanced from being aligned with the rising data edge to 90, 180 and 270 degrees.

Outputs Enable/Disable: This up/down control allows the user to select from six settings for enabling and disabling outputs during certain signal conditions. For example, if it is desired to only supply output clock and data signals if the incoming PCM signal is locked, this menu list allows the user to select this operational condition. These modes are often helpful in reducing recording data until data with substantial integrity has been obtained.

Input Selection: This control allows the user to select one of four single-ended input sources, one of two differential input sources, or an on-board TX BERT test source. If the configuration of the LS-45-B1 is for a single PCM channel, the selections will be expanded for this channel to eight single-ended input sources, four differential input sources, and an on-board TX BERT test source.

Input Impedance: This drop-down list allows the user to select four input impedances for the single-ended input ports. For differential inputs, the input impedance is 120 ohms.

Enhanced Acquisition: This control enables an enhanced acquisition mode. The mode tailors the PLL control loops and makes their reactionary rates very slow once an original acquisition cycle has been successful. This is useful when NRZ data transitions are very sparse or are non-existent for long periods. Using this mode makes reacquisition times very small because loops are nearly static once a locked signal has been obtained. Each time a new data rate is programmed, an original acquisition cycle is performed.

PCM (Tape) Output Type: This control allows the PCM Tape output types to be varied between baseband and TTL formats. A selection of this control applies to both channels, regardless of which channel's control page is used to set the control.

BERT Setup - rx BERT Enable/Disable: Each channel of the LS-45-B1 contains a Bit Error Rate Tester (BERT). This includes a pseudo-random pattern generator and

receiver. This control enables and disables the txBERT and rxBERT functions for the given channel. The BERT performance allows for error rate testing down to $1x10^{-2}$.

BERT Setup - Pattern Selection : This control allows the user to select from eighteen preset patterns. These selections are used not only in programming the on-board test source but these values are also applied to the receive BERT for correlation.

BERT Setup - Invert Data: This control allows the data being transmitted by the BERT to be inverted.

BERT Setup - Force Errors: This control allows the data being transmitted by the BERT to have forced errors. If enabled, this option will input one bit error for each pattern being generated.

BERT Setup - Reset BERT Status: This control allows the user to clear the accumulated BER status when the BERT functions are active.

Frame Sync Pattern Setup - Enabled/Disabled: Each channel of the LS-45-B1 contains a very powerful Frame Sync detector. This detector is useful in determining if a data stream contains an anticipated frame synchronization pattern. This can be used to determine if the data stream being decoded is the correct stream or act as a verification that setups are correct. The frame sync detector will automatically detect the pattern specified, and the opposite pattern.

This control enables and disables this functionality.

Frame Sync Pattern Setup - Frame Length/Frame Pattern/FSP Length/Send FSP Setup: The LS-45-B1 frame sync pattern detector has a programmable frame length in bits up to 131,072 bits, and a programmable frame sync pattern that can vary from 1 to 64 bits in length. Once configured, pressing the SEND button loads the frame synch detector.

Frame Sync Pattern Setup - Clock Invert: When enabled, this allows the Frame Sync Detector to check for the presence of inverted clocks cases when making correlation attempts.

Lumistar NetworkDevice LS45B1 BS1 General Status BS2 General Status COMB General Status Status On 00000 00000 0 0 0 0 0 BERT FSP QUAL LOCK THRES BERT FSP QUAL LOCK THRES BERT FSP QUAL LOCK THRES Fault Blink LEDs Remember Setups Es/N0: 22.48 Es/N0: 21.66 Es/N0: 22.33 Setup BS1 Setup BS2 Setup Combiner Info Bit Rate Bert Setup Bert Status rx Bert 20000000 Send 2.00 M bps Combiner Enabled PN 2^15 Errors: Pattern Selection Input PCM Code Bit Cnt: Input LBW Normal Reset Bert 0.20% Invert Data Output PCM Code Output Clk Phase Frame Sync Pattern Setup NRZ-L ♣ 0° ♣ FE6B2840 8192 32 Send FSP FSP Length Frame Sync Pattern Frame Length Tape Out PCM Code TapeOut Clk Phase Max 131,071 HEX, Most Significant Bit First NRZ-L 💠 0° 🚓 Normal Invert Clock Outputs Enable/Disable Enable all PCM Outputs (default) Frame Sync Pattern Status Lock State: @ Bit Stuffs: Frame Count: Dead Clock: 🚇 Bit Slips: Frame Length: PCM Output Type Baseband TTL

2.3.2 Combiner Controls

Figure 2-11. LS-45-B1 Combiner Dialogue

If the LS-45-B1 configuration contains the combiner option, the "Setup Combiner" tab will appear as shown in Figure 2-11. This tab contains a "Combiner Enable/Disable" button which initiates the combiner functions. This button will also result in an additional status window as shown.

When enabled, the primary PCM input controls on the combiner tab will be applied to both channels, as required for combining functions. This includes the bit rate, Input PCM code, and the Input LBW settings for each individual channel. Those controls will be disabled on both individual bit sync channel controls any time the combiner is enabled. Other independent controls for the individual channels can still be controlled in their respective tabs.

2.3.3 Info Tab

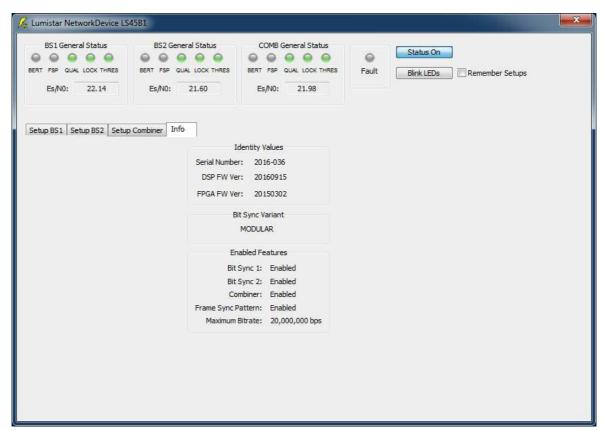


Figure 2-12. LS-45-B1 Info Tab

If the LS-45-B1 application contains an information tab which will display pertinent configuration information about the unit. An example if shown in Figure 2-12. Data contained on this tab included the firmware versions present in the design, the unit serial number, and a list of all enabled features. The maximum bit rate listed in this tab is the programmed limit of the present configuration. The true design limit is 45Mbps. The value listed in this tab may be lower than the design limit.

2.3.4 Bit Sync and Combiner Status Indications

The LS-45-B1 application provides the following status concerning the state of operations:

Fault: This indicator will be illuminated red if there is a detected hardware problem. If this indicator is illuminated, contact Lumistar customer support.

General Status - Thres: This indicator provides status of the signal level detected at the PCM input of a given channel. If the indicator is gray, the signal is below 100mVp-p. If the indicator is yellow, the detected signal level is below 400mVp-p. If the signal is above this level, the indicator will be green.

General Status - Lock: This indicator provides status of the PCM symbol lock detection state. If the indicator is gray, no symbol lock has been detected. If the level is yellow, the detected symbols do not fit all of the criteria for a locked state. If the symbols have all criteria for lock, the indicator will be green.

General Status - Qual: This indicator provides status of the PCM symbol quality. If the detected symbols have an Es/No (Energy of the Symbol/Energy of the Noise) of greater than 5dB, the indicator will be Green. If the Es/No level detected is less than 5dB, the indicator will be yellow. This indicator will only be active if the Lock state is green.

General Status - FSP: If the Frame Sync detector is enabled and locked, this indicator will be green. If the Frame Sync detector is enabled and in search, the indicator will be yellow. If the Frame Sync detector is disabled, the indicator will be gray.

General Status - BERT: If the BERT is enabled and locked, this indicator will be green. If the BERT is enabled and there are detected BER, the indicator will be yellow. If the BERT is disabled, the indicator will be gray.

General Status - Es/No: This status box provides status of the PCM symbol quality. The Es/No (Energy of the Symbol/Energy of the Noise) of the channel processing is displayed.

Extended Status - Definite/Strong/Possible/Weak 0's and 1's: These indications are percentage values of the soft bit decisions being made for incoming symbols. Each of these values gives status on the quality of the decisions being made on bits being received. As the signal SNR begins to erode, these detectors will vary. Indications that are not all in the "Definite" range does not mean that the data being decoded is in error. These are only indications of the strengths of the decisions being made.

Extended Status - Total: This status box provides the percentage of symbols detected in the last sample made.

Extended Status - Duty Cycle: This field indicates the percentage of ones and zeros detected by the bit detection engine. This will give the user a good idea of the ratio of ones being detected versus zeros.

Extended Status - Confidence: This status box provides a general signal processing confidence level in the signal processing engine providing accurate data. It is a measure of the definite detection levels. Confidence of less than 100% does NOT necessarily indicate that there are errors present in the data. This number is just an additional statistic of data being detected.

Extended Status - Transition Density: This is an indication of the transitions detected in the incoming data streams. Transitions are necessary for locking and data detection. If the count is very low, this indicates a potential for control and detection instability. This is not an indication of data ratios. It just is an indication of how many state changes were made in the latest stream of collected data.

Extended Status - Vp-p: This status box contains an estimate of the loaded signal input peak-to-peak voltage.

2.3.5 Front Panel Indications

The LS-45-B1 application provides four front panel hardware indicators concerning the state of operations:

D1 LED: D1 (Refer to Figure 1-6) will illuminate yellow when the threshold level for Channel 1 has been reached. When Channel 1 is locked, the LED will illuminate Green. When neither condition is present, the LED will be extinguished.

D2 LED: D2 (Refer to Figure 1-6) will illuminate yellow when the threshold level for Channel 2 has been reached. When Channel 2 is locked, the LED will illuminate Green. When neither condition is present, the LED will be extinguished.

D3 LED: D3 (Refer to Figure 1-6) will illuminate green when Channel 1's BERT or FSP lock states have been detected. When this condition is not present, the LED will be extinguished.

D4 LED: D4 (Refer to Figure 1-6) will illuminate green when Channel 2's BERT or FSP lock states have been detected. When this condition is not present, the LED will be extinguished.

2.3.6 BERT Status Indications

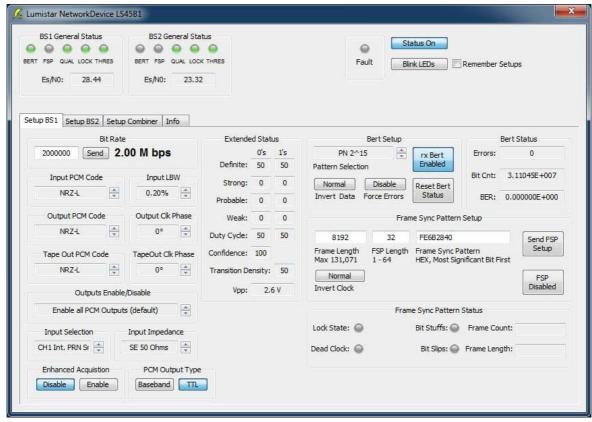


Figure 2-13. LS-45-B1 BERT Status

As shown in Figure 2-12, the LS-45-B1 application provides the following status concerning the state of operations:

Errors: This is a count of the number of errors detected by the rxBERT since the last time the BERT functions were enabled or the primary SEND button was selected.

Bit Count: This is a count of the number of bits counted since the last time the BERT functions were enabled or the primary SEND button was selected.

BER: This is a calculation of the Bit Error Rate since the last time the BERT functions were enabled or the primary SEND button was selected.

Lumistar NetworkDevice LS45B1 BS1 General Status COMB General Status Status On 00000 00000 00000 BERT FSP QUAL LOCK THRES BERT FSP QUAL LOCK THRES BERT FSP QUAL LOCK THRES Fault Blink LEDs Remember Setups Es/N0: 22.10 Es/N0: 21.90 Es/N0: 21.52 Setup BS1 Setup BS2 Setup Combiner Info Bert Status rx Bert Disabled Input PCM Code Input LBW Strong: 0 0 Normal Disable Reset Bert Invert Data Force Errors Status BER: Output PCM Code Output Clk Phase Weak; 0 0 Frame Sync Pattern Setup NRZ4. 8 0° 1 Duty Cycle: 71 29 8192 32 FE6B2840 Tape Out PCM Code TapeOut Clk Phase Confidence: 100 Frame Length FSP Length Frame Sync Pattern Max 131,071 1 - 64 HEX, Most Significan HEX, Most Significant Bit First NRZ-L 💠 0° 🖶 Transition Density: 32 Normal Invert Clock Enabled Vpp: 0.5 V Outputs Enable/Disable Enable all PCM Outputs (default) Frame Sync Pattern Status Lock State: LOCK Bit Stuffs: Frame Count: Input Impedance Input Selection CH1 SE 1 SE 50 Ohms Dead Clock: Bit Slips: Frame Length: 8192 Enhanced Acquistion PCM Output Type Disable Enable Baseband TTL

2.3.7 Frame Sync Pattern Status Indications

Figure 2-13. LS-45-B1 Frame Sync Pattern (FSP) Status

Refer to Figure 2-13 for the following paragraphs.

Lock State: This indicator will be red if the Frame Sync Detector is enabled and the lock settings have not been met. If they have been met, the indicator will be green. If the Frame Sync Detector is disabled, the indicator will be gray.

Dead Clock: If the frame sync detector is enabled and a continuous stream of data has been detected, the indicator will be gray. This indicator will be gray if the frame sync detector is disabled or when no "dead clock" condition is detected.

Bit Stuffs Present: If the frame sync detector is enabled and receives additional bits in the frame sync pattern, this indicator will be red. If the frame sync detector is enabled and receives no additional bits in the frame sync pattern, this indicator will be gray. If the frame sync detector is disabled the indicator will be gray.

Bit Slips Present: If the frame sync detector is enabled and receives too few bits in the frame sync pattern, this indicator will be red. If the frame sync detector is enabled and receives no bit slips in the frame sync pattern, this indicator will be gray. If the frame sync detector is disabled the indicator will be gray.

Frame Count: This status box will contain the present frame count detected.

Frame Length: This status box will contain the present frame length detected.