



# LS-040 D2 Series User's Manual

## Programmable Digital PCM Bit Synchronizer

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## 1. Introduction

### 1.1 General

This document is the User's Manual for the Lumistar LS-040 D2 Series Programmable Digital PCM Bit Synchronizer. The intent of this document is to provide physical, functional, and operational information for the end user.

The LS-040 D2 Series Programmable Digital PCM Bit Synchronizer provides correlated clock and data recovery from an incoming PCM stream. The LS-040 D2 provides translation of various PCM formats and provides a user programmable PCM output format, which may be used for tape storage or as a means of providing PCM format translation. The programming range of the LS-040 D2 is from 10 bps up to 25 Mbps for NRZ PCM codes and 10 bps up to 12.5 Mbps for all other supported PCM codes.

The LS-040 D2 mechanical format is that of a custom mezzanine board. In addition to the Lumistar LS-040 D2 compatible products, the LS-040 D2 card was designed to be a drop-in replacement for the SBS Technologies model 4400-TF/TM Analog Bit Synchronizer. The LS-040 D2 mechanical and interface design provides for it being directly interfaced to the following products:

- Lumistar Model LS-050 Decommutator/Simulator (VME and PCI)
- Lumistar Model LS-022 70MHz Receiver (PCI)
- Lumistar Model LS-042 Bit Synchronizer Carrier Card (VME and PCI)
- SBS Model 4422-V64 or 4422-PCI Decommutator/Simulator

In addition, the LS-040 D2 board may be used in a stand-alone role by using its auxiliary power and control interfaces.

Table 1-1 below provides specifications for electrical, mechanical, and operational characteristics of the LS-040 Programmable Digital PCM Bit Synchronizer. A block diagram of the LS-040 D2 is shown in Figure 1-1.

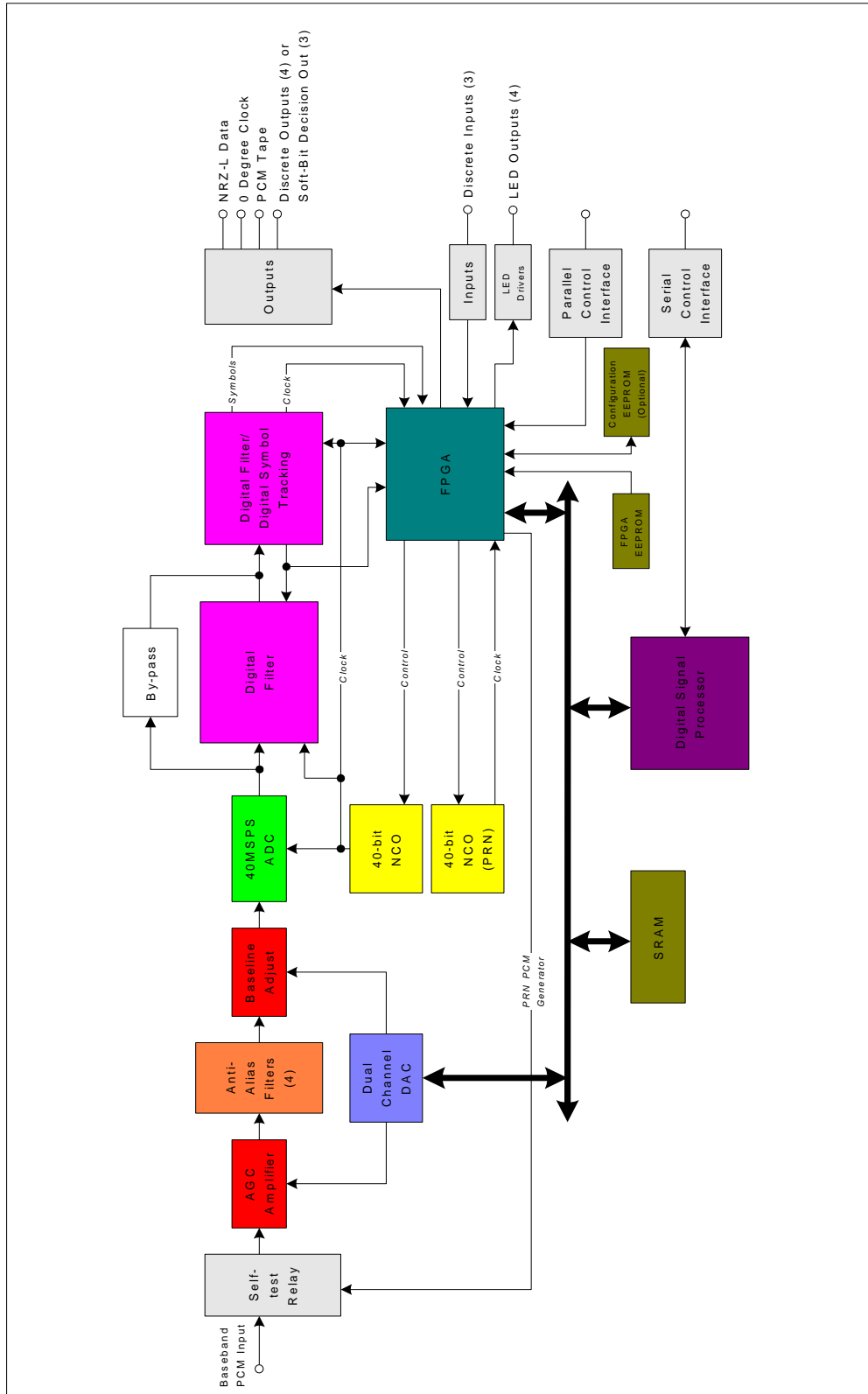
### 1.2 Manual Format

This manual is separated into the following sections:

- Chapter 1 provides a brief product overview and technical specifications.
- Chapter 2 provides LS-040 D2 theory of operation.
- Chapter 3 provides installation and configuration instructions.
- Chapter 4 provides programming information.

Category:	Specifications:	Details:
<b>Mechanical</b>		
	Envelope Dimensions	6.65"(L) x 2.85"(W) x 0.55" (H)
	Form Factor	Custom Mezzanine; Stand-alone
	Weight	< 5oz.
<b>Electrical</b>		
	Individual power requirements	+5VDC @ 1250 mA
		+12VDC @ 5.5 mA
	Total Power	< 6.33 W
<b>Inputs</b>		
	Quantity	2 – Primary: Single Ended; Auxiliary: Single Ended or Differential Input, Factory Configured
	Impedance	50, 75 or 1 K $\Omega$ ; Switch Selectable
	Rates (Option dependent)	50-20Mbps NRZ Codes; 50-10Mbps others
	Polarity	Normal or Inverse; Software Programmable
	Signal Amplitude	0.1 V to 10 V p-p
	Maximum Voltage permissible	25 V RMS
	Loop Bandwidth (LBW) settings	0.01 to 2% (data rate dependent)
	Acquisition Range	+/- (4 x LBW Setting)
	Tracking Range	+/- (10 x LBW Setting)
	Mean Acquisition Time	100-150 bits
	Discretetes	(3) TTL; <i>Consult factory for use</i>
<b>Outputs</b>		
	NRZ-L Data Output	+TTL, -TTL
	0° Clock Output	+TTL, -TTL
	PCM Output	1V p-p @ 50 $\Omega$ ; Programmable Line Codes
	PCM PRN Output	+TTL, -TTL; Programmable Line Codes
	PCM PRN Patterns	$2^{11}-1$ , $2^{15}-1$ ; Programmable
<b>Control/Status</b>		
	Parallel Command Interface	Standard PC Parallel Interface
	Serial Control/Status Interface	RS-232C Interface; Selectable BAUD rate
<b>PCM Line Codes</b>		
	Non-return to Zero Codes	NRZ-L, NRZ-M, NRZ-S
	Bi-Phase Codes	Bi $\Phi$ -L, Bi $\Phi$ -M Bi $\Phi$ -S
	Delay Modulation (Miller) Codes	DM-M, DM-S, M <sup>2</sup> M, M <sup>2</sup> S
	Return to Zero Codes	RZ
	Randomized Codes	RNRZ-L, RNRZ-S, RNRZ-M
	Randomizing Sequences	$2^{11}-1$ , $2^{15}-1$ , $2^{17}-1$ , $2^{23}-1$
<b>Environmental</b>		
	Temperature, Operational	0° to 70° C (Commercial)
	Temperature, Storage	-20° to 70° C
	Humidity, non-condensing	<40° C 0-90%, >40° C 0 to 75%

**Table 1-1** Specifications for the LS-040 D2 Series Digital Bit Synchronizer



**Figure 1-1** Block Diagram of the LS-040 D2 Series Digital Bit Synchronizer

## 2. Theory of Operation

In order to more clearly understand the operation of the LS-040 D2 Digital Bit Synchronizer, it is important to examine the general functionality and use of a bit synchronizer. The primary function of any bit synchronizer is the following:

- Receive an analog Pulse Code Modulated (PCM) input data stream.
- Adjust the incoming data stream for various signal levels and offsets.
- Filter unwanted frequencies and noise from the primary bands of interest.
- Process the data stream to recover the incoming data with a correlated clock.
- Provide the correlated clock and data output for further data processing and/or data storage.

The LS-040 D2 provides all of these functions via digital control and processing utilizing various Digital Signal Processing (DSP) technologies. This architecture provides for greater signal integrity and control and reduced operational temperature sensitivity while utilizing far less power than a traditional analog bit synchronizer. Since the LS-040 D2 contains no analog data filters, variations in performance from one unit to the next are nearly eliminated.

For the following sections, refer to the block diagram of Figure 1-1 for additional details.

### 2.1 Input Section

The input section of the LS-040 D2 Digital Bit synchronizer is composed of the following: a self-test input section relay, an input termination impedance selection, digital feed-back Automatic Gain Control (AGC) circuitry, a bank of four fixed anti-alias filters, and a digital feed-back Baseline restoration adjustment circuit.

The self-test input relay is used in conjunction with the Built-In-Test (BIT) provisions of the unit to provide switching of the on-board PRN generator test signals to the input section for power-up functional tests. More on the use of this relay is described in section 2.4.

The input termination is provided for proper impedance matching to the PCM source. Three termination impedances are provided: 50 $\Omega$  ohms, 75 $\Omega$  ohms, and 1K $\Omega$ . In addition to these typical termination impedances, additional custom termination impedance may be available. Consult the factory for availability.

Automatic Gain Control adjusts the input signal to the proper processing levels. The incoming signal may vary between 500mVp-p and 10Vp-p. The maximum input signal permissible without damage is 25V p-p. A 10-bit Digital-to-Analog Converter (DAC) channel controls the AGC circuit. Data is fed to the DAC via the Digital Signal Processing engine. The engine constantly monitors the incoming signal for variations in amplitude and adjusts the signal to the processing engine accordingly.

The signal is then passed through a bank of four fixed low-pass anti-alias filters. The anti-alias filters are used to eliminate interfering signals caused by the digital processes of the LS-040 D2. Processes of digital decimation and interpolation used by the DSP engines on the LS-040 D2 generate digital "disturbers" that can fall within the bands of interest. The anti-alias filters block these unwanted by-products from interfering with the input signals.

The final stage of the input section is a digitally controlled Baseline restoration circuit. The incoming PCM stream may be DC or AC coupled. The front end of the LS-040 D2 blocks the DC



components of the incoming stream and AC couples the signal. Slight variations due to “baseline gallop” may still interfere with the proper processing of the PCM signal. To compensate, the DSP processing engine feeds digital correction factors back to the baseline restoration circuit.

## **2.2 Digital Filtering and Processing**

Once the PCM input signal has been gain and baseline compensated by front end processing, a high-performance Analog-to-Digital Converter (ADC) is used to digitize the PCM input stream. Data is then sent through a series of digital decimation/interpolation data filtering elements followed by a digital symbol tracker. Symbol and clock information is further processed by a Field Programmable Gate Array (FPGA) to convert and decode the input PCM format.

The clock sources for the processing engine and the PRN test generator are provided via two individually controlled 40-bit Numerical Controlled Oscillators (NCOs). The two NCOs use a common precision crystal oscillator as a reference source to minimize overall jitter and drift.

## **2.3 Control, Sequencing and Memory**

At the core of the LS-040 D2 architecture is a 30 million-instruction-per-second Digital Signal Processor and a Field Programmable Gate Array (FPGA). The FPGA provides hardware control logic required by the LS-040 D2 architecture. The dedicated processor is used for overall software control and sequencing of the bit synchronizer DSP engines, direction and control of the user interfaces, as well as an interface to system memory components.

Memory on the LS-040 D2 is composed of the following: SRAM, internal DSP FLASH memory, an FPGA configuration EEPROM, and an optional serial configuration EEPROM. The processor stores the executable code of the LS-040 D2 in its internal FLASH memory. This memory is non-volatile and is **not** accessible to the user. This memory is not programmed during use and contains no operational parameter storage. SRAM is used for data variable memory storage during LS-040 D2 operation. This memory is volatile and is cleared upon loss of power. The FPGA is loaded at power-up via a serial EEPROM. This EEPROM is non-volatile and, when the optional connection is installed, is accessible to the user. The LS-040 D2 contains an (optionally configurable) serial EEPROM that stores the last valid configuration information of the LS-040 D2 such as bit rates, PCM processing codes, loop-bandwidth settings, etc. This memory is non-volatile and is automatically configured by the user writing setup information to the bit sync. As previously stated this memory is optional and can be removed for security related concerns.

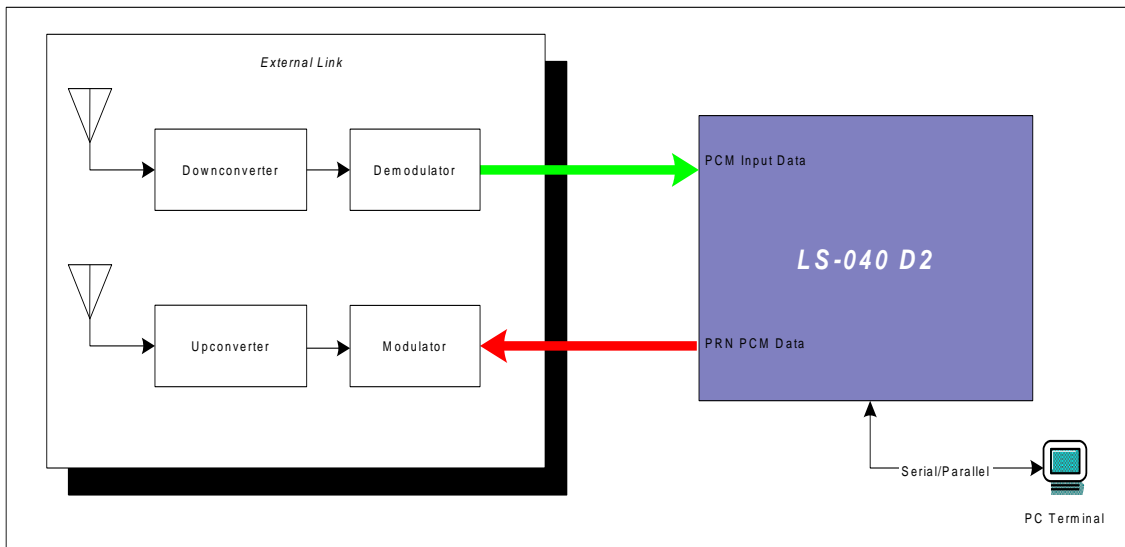
## **2.4 User Control and Status Interfaces**

The LS-040 D2 can be controlled via two interface formats. Users can interface and control the LS-040 D2 via a standard PC parallel interface bus or via an RS-232C serial interface bus. Both user interfaces provide control of the LS-040 D2. However, the serial interface bus provides additional status capabilities and controls for which no parallel interface control is provided. Consult section 4 of this manual for additional details of each of the interfaces.

## 2.5 PCM Link Analysis Functions

The LS-040 D2 provides Link Analysis functions. The link-analysis features outputs a PRN PCM pattern which can be looped internally to test the LS-040 D2 or externally to test an external PCM processing loop. This PCM output can be programmed to be any of the supported LS-040 D2 formats. The PRN pattern generator can be programmed for a pseudo-random pattern length of  $2^{11}-1$  (2,047 bits) or  $2^{15}-1$  (32,767) bits.

When using the LS-040 D2 Link-analysis functions to stimulate an external PCM processing path, the returned PCM stream is returned to the LS-040 D2 where a sliding-correlator is used to count Bit Errors and calculate Bit Error Rate (BER) performance from the external PCM link. This function is useful in determining link integrity and overall performance. Figure 2-1 below shows the interconnection of this test setup.



**Figure 2-1** PCM Link Analysis using the LS-040 D2 Series Digital Bit Synchronizer

### 3. Installation and Configuration

Chapter 3 provides installation and configuration information. This chapter will help locate serial numbers and product configuration information, familiarize the user with the layout of the board, and properly set up the hardware.

#### 3.1 Product Identification

The LS-040 D2 contains a number of configuration jumpers and a configuration switch to control various functions of the LS-040 D2. Figure 3-1 contains a diagram of the top and bottom sides of the LS-040 D2 with indications of jumper and switch locations.

The LS-040 D2 model number, serial number, revision information and product options are denoted on the rear of the board under the Lumistar, Inc. name. Figure 3-1 depicts the location of these configuration details. Consult the product data sheet for additional option configurations.

#### 3.2 Hardware Configuration

The LS-040 D2 contains a number of configuration switches to control various functions of the LS-040 D2. Figure 3-1 contains a diagram of the top and bottom sides of the LS-040 D2 with indications of jumper and switch locations.



**Warning:** The LS-040 D2 contains several hardware switches that are configured during factory test. Table 3-1 indicates which switches are factory configured. DO NOT alter these switches.

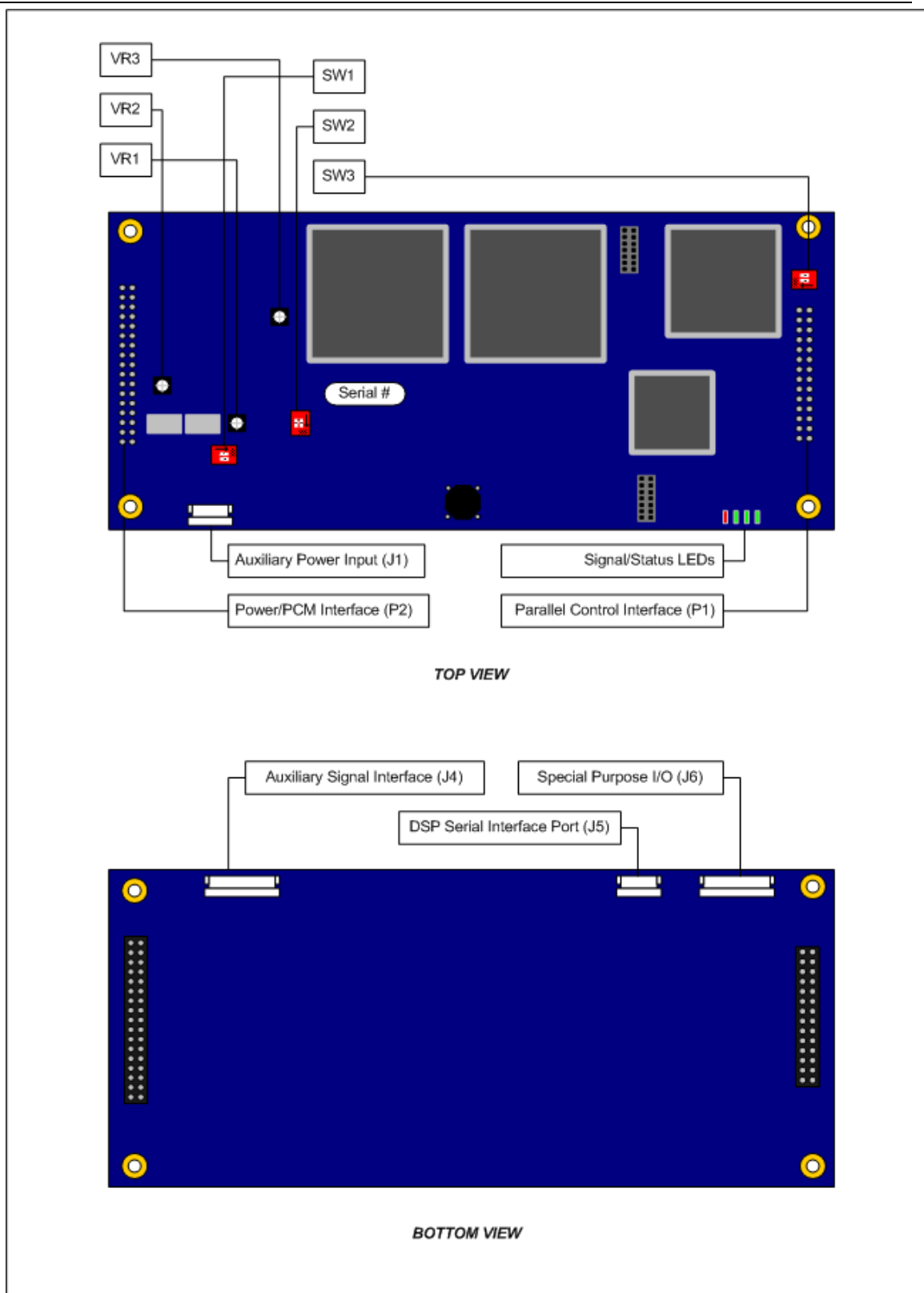


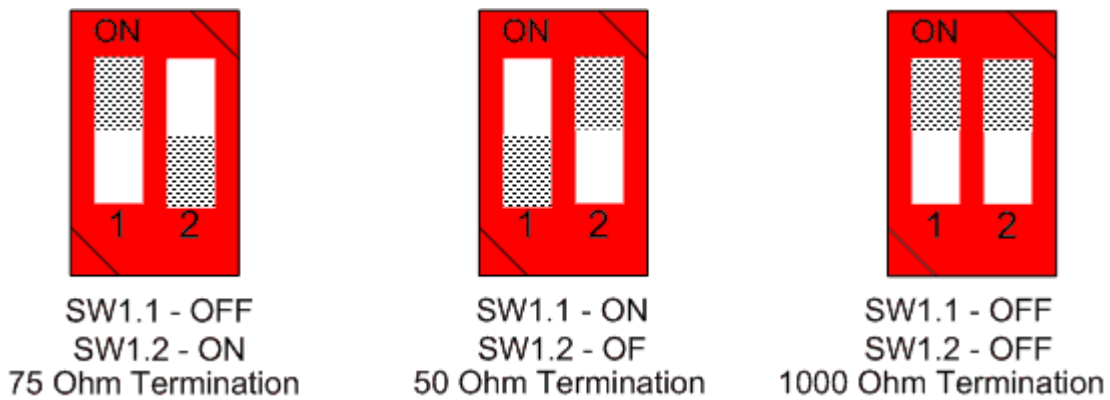
Figure 3-1 LS-040 D2 Configuration jumpers/switch locations.

All switches on the LS-040 D2 are arranged with the reference designators silk-screened near the part location. A small dot is silk-screened near pin 1 of the switch.

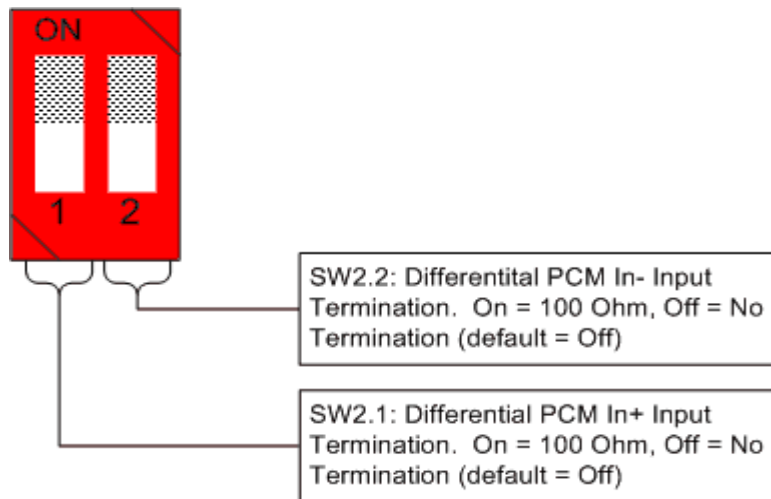
The LS-040 D2 is shipped with its switch in the configuration shown in Table 3-1. Configuration details for these jumpers are given in Figures 3-2 through 3-5.

Switch	Designation	Configuration Default	Default Selection	Reference Figure
SW1.1	Input Impedance Select		Off	3-1
SW1.2	Input Impedance Select	75 Ohm Input	On	3-1
SW2.1	Differential Input Termination	Not terminated	Off	3-2
SW2.2	Differential Input Termination	Not terminated	Off	3-2
SW3.1	JTAG Header	(Factory Use ONLY)	Off	-
SW3.2	Serial DSP Programming	(Factory Use ONLY)	Off	-

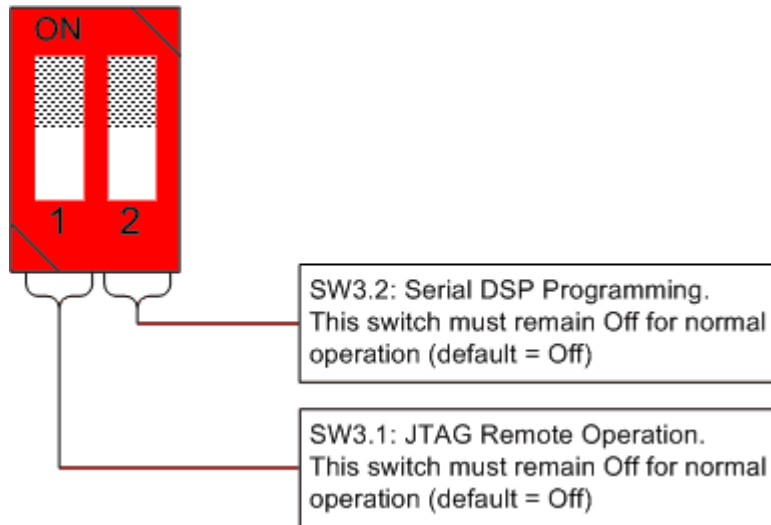
**Table 3-1** LS-040 D2 Default Switch Configurations



**Figure 3-1** LS-040 D2 Single-Ended (SE) Input Termination Configuration Switches



**Figure 3-2** LS-040 D2 Differential Input Termination Configuration Switches



**Figure 3-3** LS-040 D2 DSP Programming Modes

### 3.3 Physical Installation

To install the LS-040 D2, the following procedure should be followed:

1. Perform normal system shutdown of the PC system and remove the primary power plug.
2. Remove or obtain the unit on which the LS-040 D2 is to be mounted.
3. Orient the LS-040 D2 with the P1 and P2 Mounting connectors positioned over the mating connectors. The mounting holes at the corners of the LS-040 D2 should align with the stand-offs used for securing the device.
4. Install the mounting screws at the corners of the device to secure the unit.



**Warning:** The interface pins of the LS-040 D2 are fragile. Insure that the interface connectors are properly aligned prior to installation to prevent pin fractures.

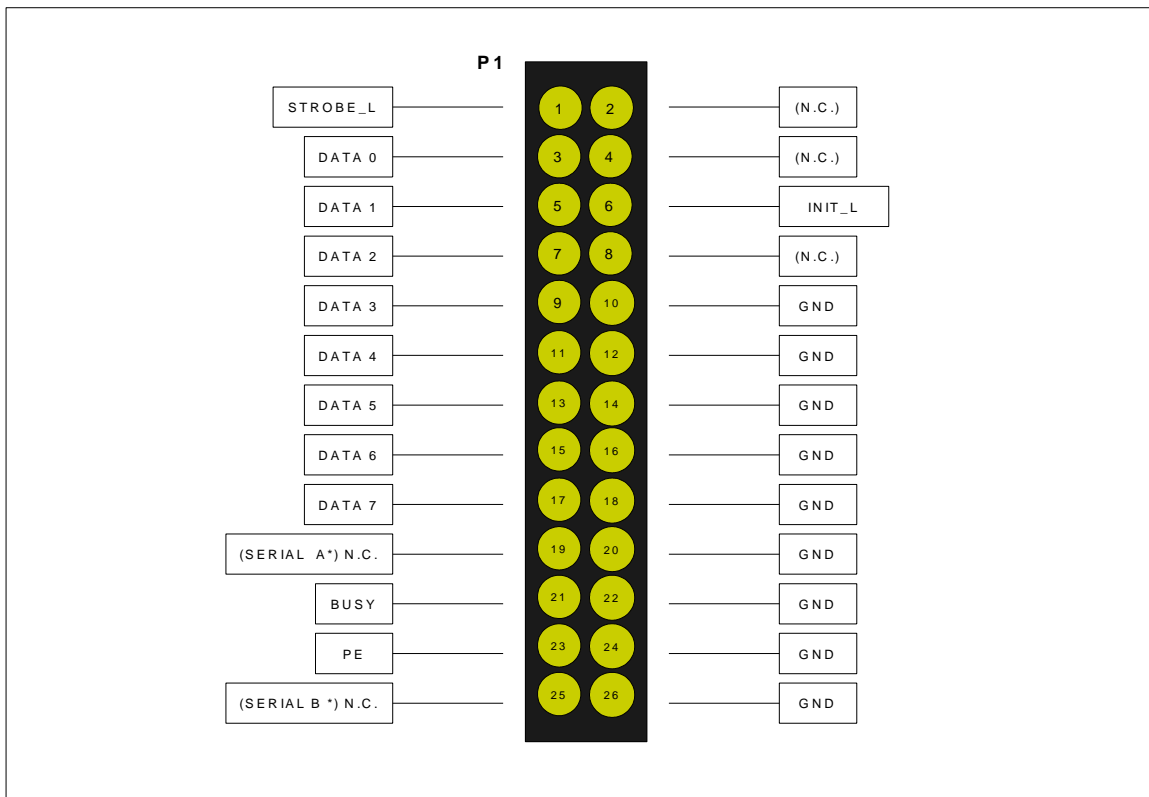
### 3.4 Interconnection

The LS-040 D2 provides six user interface connectors. In the standard configuration, only the P1 and P2 connectors are required for interfacing the LS-040 D2 to its intended host. For additional functionality, and for stand-alone operation, four additional interface connectors are provided. Table 3-3 provides mating connector information for all interface connectors of the LS-040 D2.

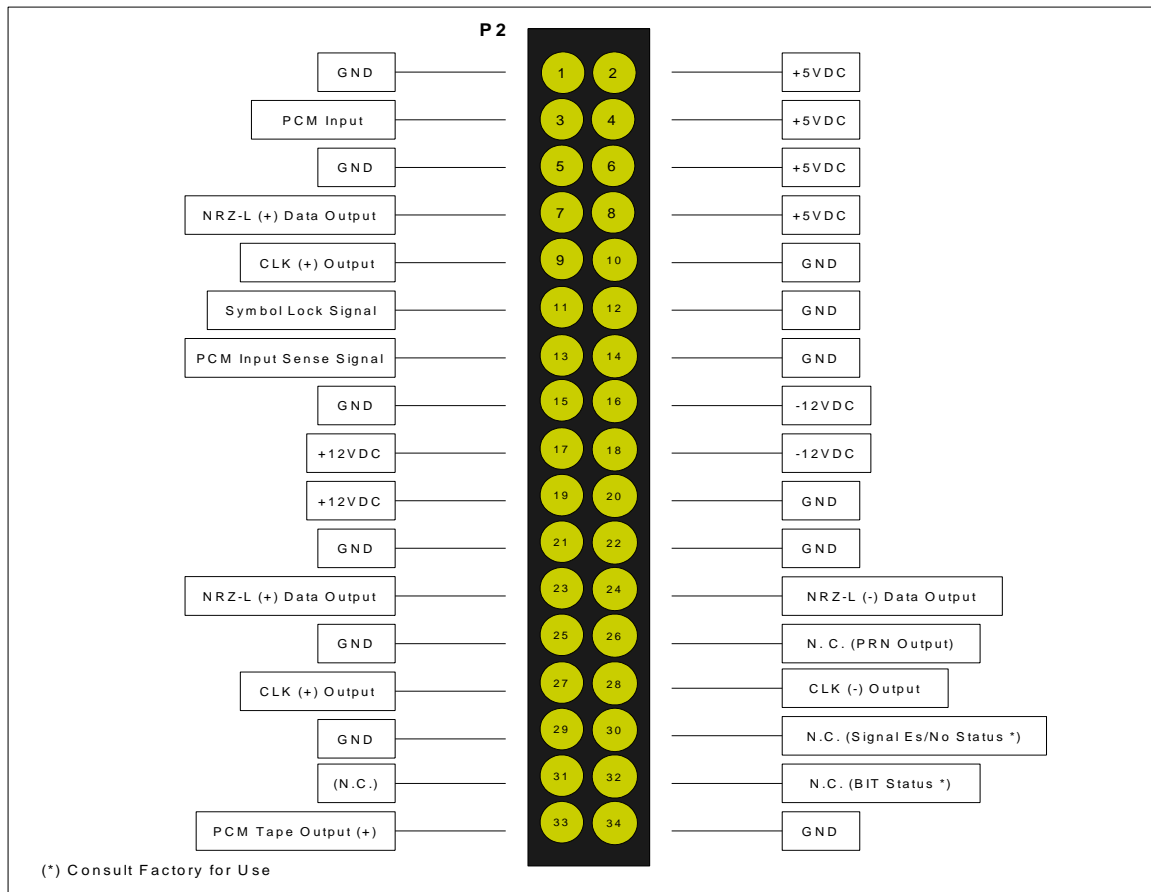
Figures 3-7 and 3-8 provide interface pin-outs for the P1 and P2 connectors. Tables 3-4 and 3-5 provide pin-out details for the auxiliary PCM interface connector J1 and serial auxiliary connector J3 respectively. Table 3-6 provides pin-out information for the stand-alone auxiliary power connector J2. Figure 3-9 provides pin-out information for the auxiliary external status LED output connector JP1 and the status LED definitions.

Connector	Function	Mating Connector Part No.	Manufacturer
P1 (0.018 Pins)	Command Bus Interface	SD-113-G-2	Samtec
P1 (0.025 Pins)	Command Bus Interface	SSW-113-01-G-D	Samtec
P2 (0.018 Pins)	PCM and Power Interface	SD-117-G-2	Samtec
P2 (0.025 Pins)	PCM and Power Interface	SSW-117-01-G-D	Samtec
J1	Auxiliary Power Input		Molex
J2	Xilinx JTAG Chain Connector		
J3	DSP JTAG Connector		
J4	Auxiliary Signal Interface		Molex
J5	Serial Interface Port		Molex
J6	Special Purpose I/O		Molex
-	Terminals, J1/J3 Connector	50641-8141	Molex
-	Terminals, J2 Connector	08-50-0114	Molex
-	Crimp tool for J1/J3 Term.	57352-5000	Molex

**Table 3-3** LS-040 D2 Mating Connectors



**Figure 3-4** LS-040 D2 (P1) Parallel Interface Control Connector



**Figure 3-5** LS-040 D2 (P2) PCM and Power Connector

<i>Pin Number</i>	<i>Function</i>
J1-1	PCM Input (+)
J1-2	PCM Input (-)
J1-3	Ground
J1-4	Clock Out (+)
J1-5	Clock Out (-)
J1-6	Ground
J1-7	NRZ-L Data Out (+)
J1-8	NRZ-L Data Out (-)
J1-9	Ground
J1-10	PCM Encoder Output (+)
J1-11	PCM Encoder Output (-)
J1-12	Ground
J1-13	PRN PCM Generator Output (+)
J1-14	PRN PCM Generator Output (-)

**Table 3-4** LS-040 D2 Auxiliary PCM Interface Connector Pin-out

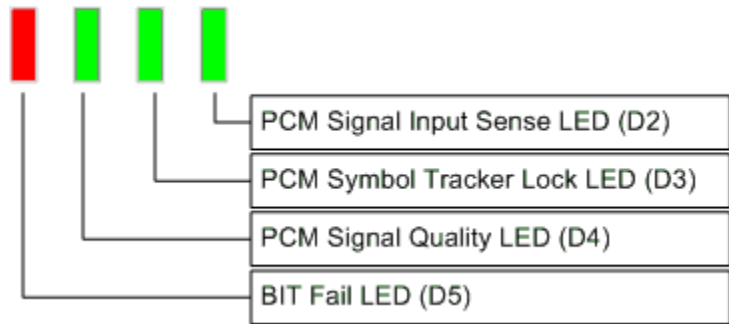


<i>Pin Number</i>	<i>Function</i>
J3-1	Special Function Input1
J3-2	Ground
J3-3	Special Function Input 2
J3-4	Ground
J3-5	Special Function Input 3
J3-6	Special Function Output 1 / Soft Decision D0
J3-7	Ground
J3-8	Special Function Output 2 / Soft Decision D1
J3-9	Special Function Output 3 / Soft Decision D2
J3-10	Ground
J3-11	Special Function Output 4
J3-12	Serial Interface A
J3-13	Ground
J3-14	Serial Interface B

**Table 3-5** LS-040 D2 Auxiliary I/O Interface Connector Pin-out

<i>Pin Number</i>	<i>Function</i>
J1-1	+12VDC
J1-2	Ground
J1-3	Ground
J1-4	Ground
J1-5	+5VDC

**Table 3-6** LS-040 D2 Auxiliary Power Connector Pin-out



**Figure 3-6** LS-040 D2 Signal LED Definitions

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## 4. Programming

This chapter provides LS-040 D2 programming and setup information. The LS-040 D2 provides control and status interfaces via two hardware formats: an IEEE 1284-style bi-directional PC parallel interface and an EIA232 (RS-232) serial interface. Both interfaces use the same command formatting and command set. Provisions for programming multiple devices with one host interface will also be described in the following paragraphs.

### 4.1 Interface Command Set

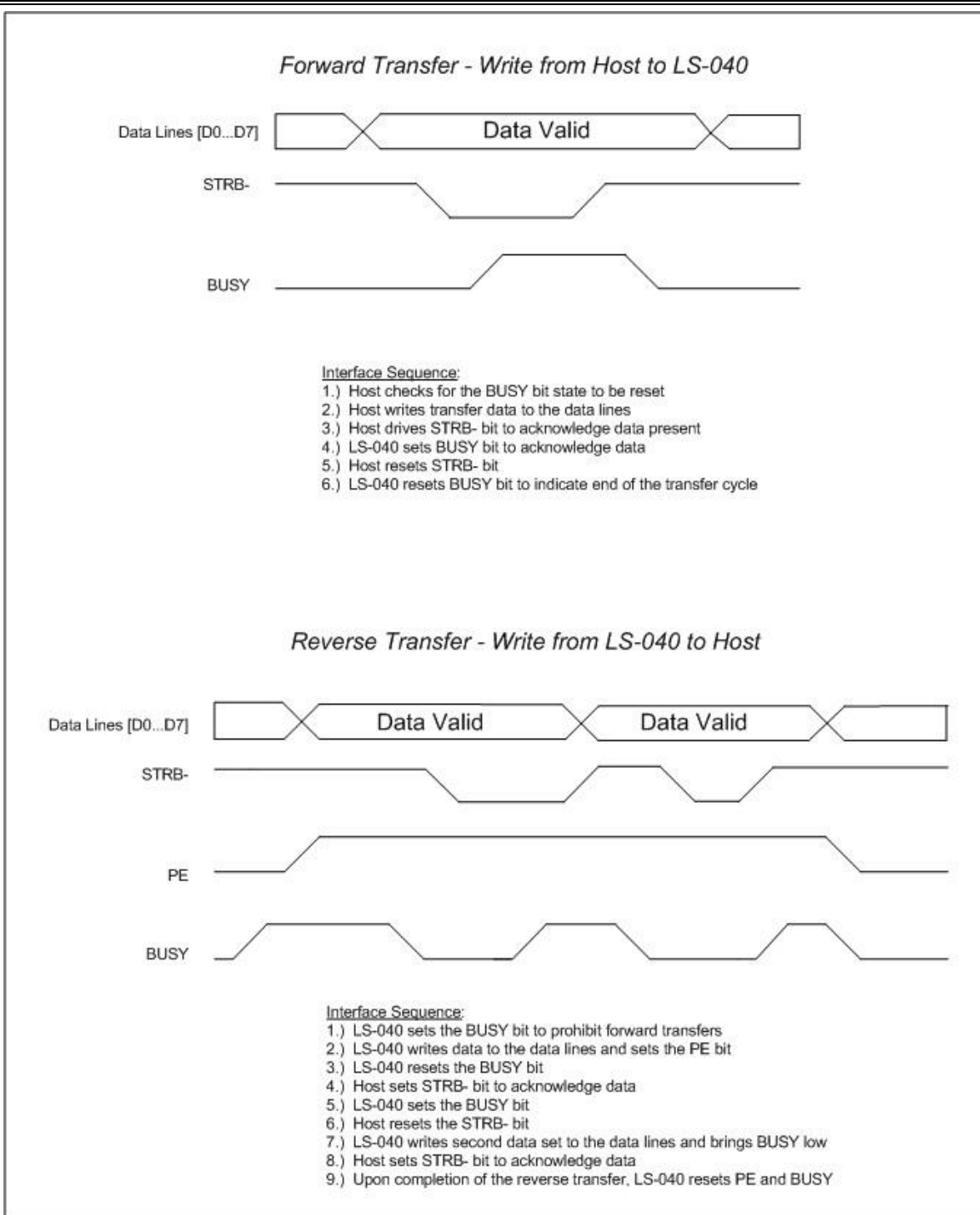
The LS-040 D2 can be **commanded** via a standard PC bus interface or via the native host interfaces of the following devices: Lumistar LS-050 or LS-022 series products, or the SBS 4422 series products. In addition, a standard PC bus architecture or the host interfaces of the Lumistar LS-050 or LS-022 series products can be used to obtain operational **status** from the LS-040 D2. The interface command set maintains compatibility with the existing interface definitions for the SBS 4400-series command set and makes some additions to the set to allow for additional features of the LS-040 D2. A few of the existing commands have been redefined or are not applicable to the LS-040 D2 design. Table 4-1 provides commands definitions for both the LS-040 D2 and the corresponding commands for the SBS 4400-TF series interface. Paragraphs in section 4.2 of this document provide further detail of command definitions.

Command (Hex)	Command Category	Lumistar LS-040 Function	Reference Section
0x0_	Control	General Operational Setup Commands	4.2.1
0x9_	Control	PCM Bit Rate Commands (x10 Mbps) [0..2 range]	4.2.2
0x1_	Control	PCM Bit Rate Commands (x1 Mbps) [0..9 range]	4.2.2
0x2_	Control	PCM Bit Rate Commands (x100kbps) [0..9 range]	4.2.2
0x3_	Control	PCM Bit Rate Commands (x10kbps) [0..9 range]	4.2.2
0x4_	Control	PCM Bit Rate Commands (x1kbps) [0..9 range]	4.2.2
0x5_	Control	PCM Bit Rate Commands (x100bps) [0..9 range]	4.2.2
0x6_	Control	PCM Bit Rate Commands (x10bps) [0..9 range]	4.2.2
0x7_	Control	PCM Bit Rate Commands (x1bps) [0..9 range]	4.2.2
0x8_	Control	Tentative Loop Bandwidth Commands	4.2.3
0xA_	Control	Primary PCM Decoder Commands	4.2.4
0xB_	Control	Primary PCM Encoder Commands	4.2.5
0xC_	Control	Auxiliary Commands	4.2.6
0xD_	Control	Secondary PCM Decoder/Encoder Commands	4.2.7
0xE_	Status	Status Commands	4.2.8
0xF_	Address	Reserved for Airborne option	4.2.9

Table 4-1 LS-040 Interface Command Set

#### 4.1.1 Command Formats

The LS-040 D2 provides for a bi-directional “master-slave” command and status interface. When using the IEEE 1284-style interface bus, interface control is maintained by the use of a “handshake” back to the commanding host via the BUSY discrete (See Figure 3-7, connector P1, pin 22). The host MUST wait until the BUSY bit is returned low prior to issuing additional commands to prevent commands from being missed. Figure 4-1 depicts the sequence of signal events that occur in both forward and reverse transmissions between the LS-040 and the host.



**Figure 4-1** LS-040 D2 IEEE 1284 Bi-directional Interface Command Signal Sequences

When utilizing the EIA232 standard interface, the LS-040 D2 monitors all asynchronously transmitted traffic from the commanding host without the use of a handshake signal. Command responses are transmitted back to the host via a separate signal path from the LS-040 D2 to the host. Commands from the host are provided a higher priority than that of the status responses from the LS-040 D2.

The LS-040 D2 decodes and processes commands via either bus interface and responds in accordance to the command set described in Table 4-1. Commands may be transmitted individually or in a group. In order to activate a particular command, or group of commands, the "*Master Configuration*" command (0x0A) must be transmitted as the last command in the sequence. The "*Master Configuration*" command tells the LS-040 D2 internal software to gather up all changes that it received since its last update and apply them and/or to form a response to a requested action. Figure 4-2 depicts the command set sequencing and responses from the LS-040 D2.

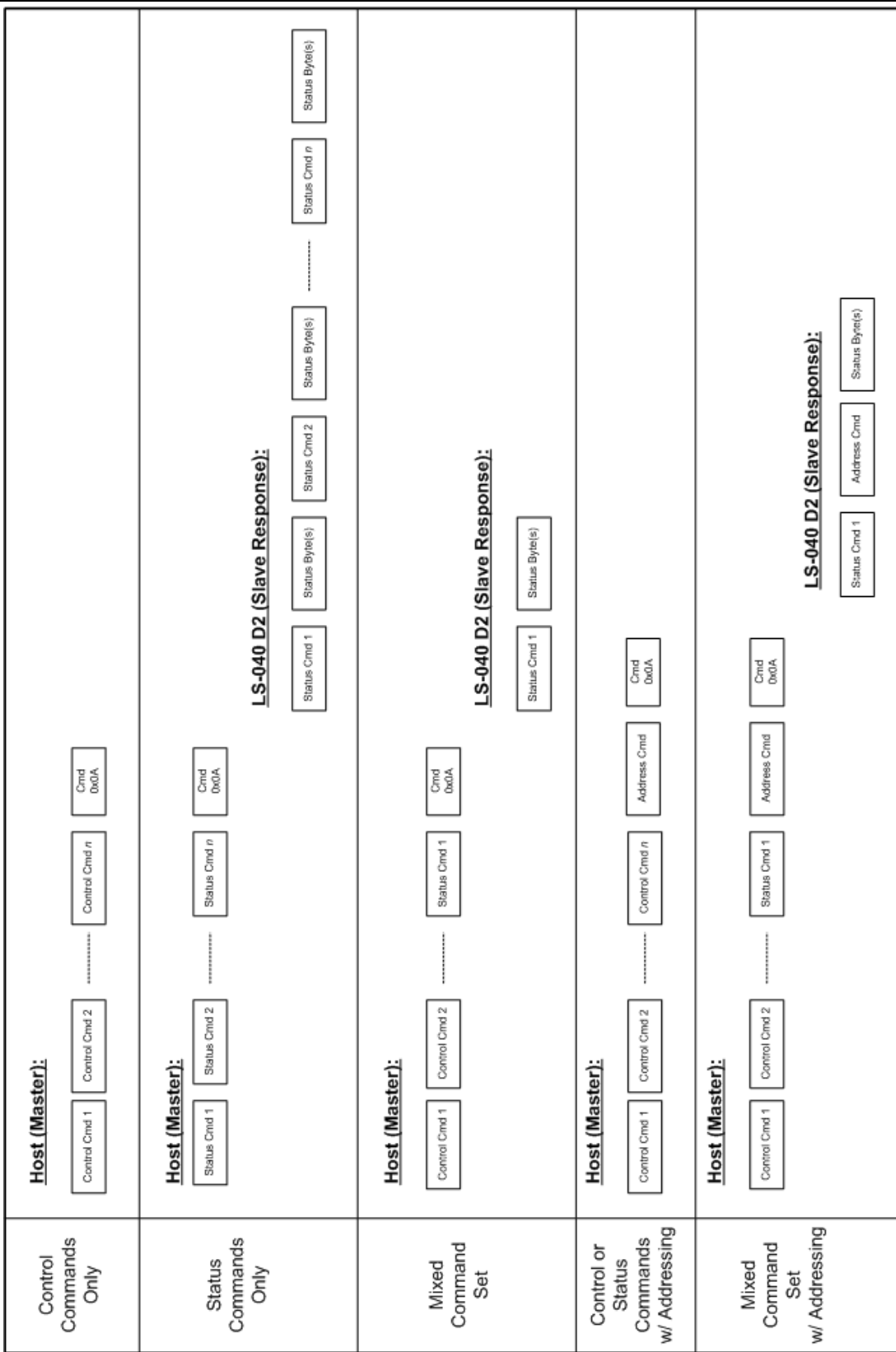


Figure 4-2 LS-040 D2 Command Sequencing

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## 4.1.2 Invalid, Undefined or Reserved Command Processing

The LS-040 D2 has a defined set of commands for which it will respond. Commands may inadvertently be sent which are undefined or invalid. If this should occur, the LS-040 D2 will ignore these commands and continue with the processing of the additional commands.

## 4.1.3 Configuration EEPROM Storage

The LS-040 D2 contains an on-board configuration EEPROM, which is factory-defaulted to be disabled. As an option, the factory can enable the EEPROM for reading and writing. This EEPROM is used to store the last valid setup of the bit synchronizer variables. This is particularly useful for stand-alone operation where the unit needs to power-up in its last known configuration.

If the EEPROM option is enabled, the configuration EEPROM will automatically retrieve the last valid LS-040 D2 setup criteria at power-up. While in operation, any changes to the LS-040 D2 operational setup will automatically be stored in EEPROM.

## 4.2 Command Details

The following sections detail the individual commands, status responses and their associated functions.

### 4.2.1 General Operational Setup Commands (0x0\_)

The LS-040 D2 provides a set of general operational setup commands that maintain that enable and disable the main operating functions for the device. Table 4-2 lists these commands and their associated reference paragraphs that explain the commands in greater detail.

General Setup Commands	Function	Reference Section
0x00	(Undefined)	
0x01	(Undefined)	
0x02	(Undefined)	
0x03	EEPROM Write Command	
0x04	Disable Enhanced Acquisition Mode	4.2.1.1
0x05	Use Frame Sync Method to determine Signal Quality	
0x06	Use Original Method of determining Signal Quality	
0x07	(Undefined)	
0x08	Enable RRC Filtering	4.2.1.2
0x09	Enable I&D Bit Decision Methods	4.2.1.2
0x0A	Master Configuration Command	4.2.1.3
0x0B	(Undefined)	
0x0C	(Undefined)	
0x0D	(Undefined)	
0x0E	Enable Enhanced Acquisition Mode	4.2.1.1
0x0F	(Undefined)	

**Table 4-2** LS-040 D2 General Operational Commands

#### **4.2.1.1 Enhanced Acquisition Mode Enable/Disable (0x04 and 0x0E)**

The LS-040 D2 normally operates in an Integrate and Dump (I&D) mode which is closely controlled and monitored via the internal digital filtering and symbol tracking engines. In certain operational circumstances during the use of NRZ PCM code, long strings of ones or zeros in the data stream (i.e. an idle data period longer than 1024 bits) may cause the tracking engines to inadvertently begin an input signal acquisition phase. Since the switch from symbol tracking to symbol acquisition modes includes the adjustment of the processing engines coarse and fine AGC tracking, as well as frequency sweeping outside of the programmed loop bandwidth, the sudden resumption of data transitions may cause a period of corrupt data.

To counter this situation, the LS-040 D2 includes an “enhanced acquisition mode”. When enabled, the LS-040 D2 will determine when the internal stream is locked to a data source and then severely restrict both the AGC actions and frequency sweeping allowing it to quickly resume lock (typically in less than 50 bits) after long periods of idle data.



**Warning:** The Enhanced Acquisition Mode should be disabled for most operational scenarios. See the following paragraph for more details.

This enhanced acquisition mode requires that the initially locked data stream maintain an Es/No level of greater than 5dB for a period of 10000 bits. If the data quality of the initially locked signal is poor, this mode may have an undesirable effect. This mode would not be suggested for signal streams with a large amount of frequency drift.

#### **4.2.1.2 EEPROM Write Command (0x03)**

#### **4.2.1.3 Enable/Disable Frame Sync Signal Quality (0x05 and 0x06)**

The LS-040 D2 can optionally be configured at the factory to recognize a PCM Frame Synchronization Pattern and replace the Signal Quality signal with this alternate signal. If this feature is enabled, the 0x05 command is used to define the Frame Sync parameters and turn on the feature. The 0x06 command is used to revert the LS-040 D2 to use the original Signal Quality signal.

A typical setup command would be the command 0x05, followed by 8 more bytes (64 bits) of Frame Sync Pattern, left aligned and eldest bit first, followed by a byte containing the Frame Sync Pattern length (valid values between 1 and 64), followed by a byte containing the tolerance value (valid values are between 0 and 14), followed by two bytes containing the total Frame Sync Length in bits, most significant byte first, followed by the 0x0A Master Configuration Command. For a PCM stream that used a Frame Sync Pattern of FE682840h with a frame size of 4096 bits would send the following bytes: 0x05 0xFE 0x68 0x28 0x40 0x00 0x00 0x00 0x00 0x20 0x00 0x10 0x00 0x0A. Note that once a 0x05 command is sent, the following 12 bytes sent will be interpreted as FSP setup data. You may not intersperse other commands within the 12 bytes following the 0x05 command, however you may place other commands between the last byte of FSP setup data and the 0x0A Master Configuration Command.

This feature is only available when the LS-040 D2 is programmed to have 0x41 or 0x42 for its Parallel Port ID. If that is true and the factory has enabled the LS-040 D2 to allow Frame Sync Signal Quality, then the EEPROM location at Page 1 and Line 5 will be set to 0x0001 or greater. If the feature is not allowed, the value at that EEPROM location will be 0x0000.

#### **4.2.1.4 I&D and RRC Commands (0x08 and 0x09)**

The LS-040 D2 normally operates in an Integrate and Dump (I&D) mode during typical operations. This can be command using the “*Enable I&D Bit Decision Method*” command (0x09). If more rounded data is expected, an addition Raised-Root Cosine (RRC) filter can be applied to the data by commanding the “*Enable RRC Filtering*” command (0x08). This is commonly referred to as the “Filter Sample” method. In most operational environments, invoking the RRC filter option is not necessary.

These two commands are mutually exclusive. Only one of these commands is active at a given time. Either the LS-040 D2 is operating in an I&D mode without the use of the RRC filter, or the LS-040 is operating in an I&D modes with the RRC filter enabled.

#### **4.2.1.5 Master Configuration Command (0x0A)**

The “*Master Configuration Command*” (0x0A) is used by the LS-040 D2 to indicate that a command sequence is complete and to act on the commands that it has received. The commanding host MUST issue this command at the end of a command sequence to enact the desired changes.

#### **4.2.2 PCM Bit Rates Commands (0x1\_ through 0x7\_ and 0x9\_)**

The LS-040 D2 10Mbps Model is capable of processing from 10bps to 10Mbps in NRZ PCM formats (10bps to 5Mbps all other formats) and the LS-040 D2 20Mbps model is capable of processing from 10bps to 20Mbps in NRZ PCM formats (10bps to 10Mbps in all other PCM formats). Commanded data rates are programmed by a series of bit rate grouped commands based on powers of 10.

As an example, the command sequence for commanding the LS-040 D2 to a bit rate of 10,575,000 is shown below:

<u>Bit Rate Position</u>		<u>Formula</u>	<u>Command Set</u>
10,000,000	=	1x 10Mbps	0x91
1,000,000	=	0x 1Mbps	0x10
100,000	=	5x 100kbps	0x25
10,000	=	7x 10kbps	0x37
1,000	=	5x 1kbps	0x45
100	=	0x 100bps	0x50
10	=	0x 10bps	0x60
1	=	0x 1bps	0x70
			0x0A (Master Configuration Command)



### 4.2.3 Tentative Loop Bandwidth Commands (0x8\_)

The LS-040 D2 allows the user to program the loop bandwidth (LBW) based on the expected input signal. A larger loop bandwidth setting allows the bit synchronizer a larger tracking and acquisition range for less stable or more noise prone signals. Lower loop bandwidths are used for enhanced performance on more tightly controlled input signals.

Programming of the LBW setting is considered tentative. The user may elect to program any loop bandwidth that they desire. However, there are practical tracking and acquisition limits imposed by the LS-040 D2 symbol tracker design. As an example, if a 2% LBW selection were programmed at a bit rate of 20Mbps, the loop would extend +/-400 kHz around the desired input signal. The acquisition loop extends this loop to 4 times the LBW setting making the acquisition loop 1.6MHz. Due to practical limitations of the digital filters, this is beyond the programmable range for high data rates. Regardless of the commanded LBW setting, on-board software of the LS-040 D2 will default the maximum bandwidth settings according to the values in Table 4-3. Table 4-4 provides a chart of commands for both the LS-040 D2 and the corresponding setting for the SBS 4400-TF.

Bit Rate Range	Maximum LBW Setting
50bps ≤ Bit Rate < 400,010bps	2%
400,010bps ≤ Bit Rate < 800,010bps	1%
800,010bps ≤ Bit Rate < 1,600,100bps	0.5%
1,600,100bps ≤ Bit Rate < 3,200,100bps	0.2%
3,200,100bps ≤ Bit Rate < 5,000,100bps	0.1%
5,000,100bps ≤ Bit Rate < 10,001,00bps	0.05%
10,001,000bps ≤ Bit Rate < 20,000,00bps	0.02%

**Table 4-3** LS-040 D2 Maximum LBW Settings based on programmed bit rate

Loop Bandwidth (LBW) Commands	LS-040 Setting	SBS 4400-TF Setting
0x80	(Invalid)	(Invalid)
0x81	0.1%	0.1%
0x82	0.2%	0.2%
0x83	0.2%	0.3%
0x84	0.2%	0.4%
0x85	0.5%	0.5%
0x86	0.5%	0.6%
0x87	0.5%	0.7%
0x88	1.0%	0.8%
0x89	1.0%	0.9%
0x8A	1.0%	1.0%
0x8B	2.0%	2.0%
0x8C	2.0%	3.0%
0x8D	0.01%	(Invalid)
0x8E	0.02%	(Invalid)
0x8F	0.05%	(Invalid)

**Table 4-4** LS-040 D2 Commands for LBW Settings

#### 4.2.4 Primary PCM Decoder Commands (0xA\_)

The LS-040 D2 allows the user to program the PCM input decoder for a variety of input formats. The PCM decoder is used to translate the incoming PCM format to the provided NRZ-L output data format. Table 4-5 lists the PCM decoder setup commands.

PCM Input Decoder Commands	Function
0xA0	Command PCM Input Decoder to NRZ-L
0xA1	Command PCM Input Decoder to NRZ-M
0xA2	Command PCM Input Decoder to NRZ-S
0xA3	Command PCM Input Decoder to BiΦ-L
0xA4	Command PCM Input Decoder to BiΦ-M
0xA5	Command PCM Input Decoder to BiΦ-S
0xA6	Command PCM Input Decoder to DM-M
0xA7	Command PCM Input Decoder to DM-S
0xA8	Command PCM Input Decoder to Modified DM-M
0xA9	Command PCM Input Decoder to Modified DM-S
0xAA	Command PCM Input Decoder to Inv. NRZ-L
0xAB	Command PCM Input Decoder to Inv. BiΦ-L
0xAC	Command PCM Input Decoder to RZ
0xAD	Command PCM Input Decoder to Inv. RZ
0xAE	Command PCM Input Decoder to RNRZ-11
0xAF	Command PCM Input Decoder to RNRZ-15

Table 4-5 LS-040 Commands for Primary PCM decoder settings

#### 4.2.5 Primary PCM Encoder Commands (0xB\_)

The LS-040 D2 allows the user to program the PCM output encoder for a variety of PCM output formats. The PCM encoder is used to translate the incoming PCM format to another desired PCM output data format. This is helpful for tape storage or may be used to accomplish PCM-to-PCM translation tasks. Table 4-6 lists the PCM encoder setup commands.

PCM Input Decoder Commands	Function
0xB0	Command PCM Output Encoder to NRZ-L
0xB1	Command PCM Output Encoder to NRZ-M
0xB2	Command PCM Output Encoder to NRZ-S
0xB3	Command PCM Output Encoder to BiΦ-L
0xB4	Command PCM Output Encoder to BiΦ-M
0xB5	Command PCM Output Encoder to BiΦ-S
0xB6	Command PCM Output Encoder to DM-M
0xB7	Command PCM Output Encoder to DM-S
0xB8	Command PCM Output Encoder to Modified DM-M
0xB9	Command PCM Output Encoder to Modified DM-S
0xBA	Command PCM Output Encoder to Inv. NRZ-L
0xBB	Command PCM Output Encoder to Inv. BiΦ-L
0xBC	Command PCM Output Encoder to RZ
0xBD	Command PCM Output Encoder to Inv. RZ
0xBE	Command PCM Output Encoder to RNRZ-11
0xBF	Command PCM Output Encoder to RNRZ-15

Table 4-6 LS-040 Commands for Primary PCM encoder settings

## 4.2.6 Auxiliary Commands (0xC\_)

The LS-040 D2 provides a set of auxiliary commands that allows for additional features of the LS-040 to be enabled or disabled. Table 4-7 Lists these functions and associated reference paragraphs that explain the commands in greater detail.

Auxiliary Commands	Function	Reference Section
0xC0	Disable Auto-test at startup	4.2.6.1
0xC1	Enable Auto-test at startup	4.2.6.1
0xC2	PRN generator providing 2 <sup>11</sup> -1 pattern sequence	4.2.6.2
0xC3	PRN generator providing 2 <sup>15</sup> -1 pattern sequence	4.2.6.2
0xC4	PCM Outputs Disabled at PLL UNLOCK	4.2.6.3
0xC5	PCM Outputs Disabled at Es/No < 5dB	4.2.6.3
0xC6	PCM Encoder Output Disabled at PLL UNLOCK	4.2.6.3
0xC7	PCM Encoder Output Disabled at Es/No < 5dB	4.2.6.3
0xC8	Enable All PCM Output Sources	4.2.6.3
0xC9	Disable Link Analysis	4.2.6.4
0xCA	Enable Link Analysis	4.2.6.4
0xCB	Disable Link Analysis Forced Error	4.2.6.5
0xCC	Enable Link Analysis Forced Error	4.2.6.5
0xCD	Select Primary Input	4.2.6.4
0xCE	Enable Internal Link Analysis/Select PRN Generator Input	4.2.6.4
0xCF	Select Auxiliary Input	4.2.6.4

**Table 4-7** LS-040 D2 Auxiliary Function Commands

### 4.2.6.1 Disable/Enable Auto-test Commands (0xC0 and 0xC1)

At the initiation of power to the LS-040 D2, the unit initiates several Built-In-Test (BIT) functions. One of these tests wraps the on-board PRN generator to the PCM input of the device. This in turn tests the functionality of over 95% of the LS-040 D2 components. However, this period of testing disables the PCM input channel for several seconds. In some circumstances, a user may wish to disable this feature. The “*Disable Auto-test at Startup*” command (0xC0) disables this feature. The “*Enable Auto-test at Startup*” command (0xC1) enables this feature.

The LS-040 D2 is shipped from the factory with this feature enabled. For most users, it is recommended that this feature remain enabled during normal use. The Auto-test feature completes long before most operating systems can establish normal control.

### 4.2.6.2 PRN Generator Pattern Commands (0xC2 and 0xC3)

The LS-040 D2 has a built-in Pseudo-Random Number (PRN) generator that is used to drive a PCM output channel used for self-test functions as well as for performing link-analysis functions. The user is allowed to select the PRN “seed” function which determines the length of the PRN pattern that generator will sequence through before repeating. On the LS-040 D2, there are two different pattern lengths: 2<sup>11</sup>-1 (2,047 bits) and 2<sup>15</sup>-1 (32,767 bits).

The user is allowed to select either pattern format by sending the “*PRN generator providing 2<sup>11</sup>-1 pattern sequence*” command (0xC2) or the “*PRN generator providing 2<sup>15</sup>-1 pattern sequence*” command (0xC3). The LS-040 defaults to the 2<sup>11</sup>-1 PRN pattern sequence if not otherwise commanded.

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#### **4.2.6.3 PCM, NRZ-L Clock and Data Output Controls (0xC4 through 0xC8)**

In certain operational environments, it may be desirable to disable all PCM output sources, or just the LS-040 D2's PCM encoder output if the bit sync is no longer locked or if the quality of the signal is very poor. In order to allow for this feature, the LS-040 D2 provides four commands which will disable the clock, data and PCM Encoder outputs: "PCM Outputs Disabled at PLL UNLOCK" command (0xC4), the "PCM Outputs Disabled at Es/No <5dB" command (0xC5), the "PCM Encoder Output Disabled at PLL UNLOCK" command (0xC6), and the "PCM Encoder Output Disabled at Es/No <5dB" command (0xC7). Poor quality of the input signal is defined as an Es/No level of 5dB or less. PLL unlock is defined as periods when the symbol processing engine leaves the input signal tracking state and enters the acquisition state. The user can disable the data sources if the estimated PCM input signal-to-noise ratio Es/No is below 5dB or if the PLL of the bit sync has entered a symbol acquisition (unlocked) state.

The default startup state is to have all PCM output sources enabled. LS-040 D2 is shipped from the factory with this feature disabled.

#### **4.2.6.4 Enable/Disable Link Analysis (0xC9 and 0xCA), Input Select (0xCD, 0xCE and 0xCF)**

The Enable/Disable Link Analysis and the Input Select commands are related.

The LS-040 D2 has the capacity to select between two separate external inputs, the Primary Input and the Auxiliary Input, and an internal PRN Generator. The Auxiliary Input can be configured at the factory to be a single-ended or a differential input. A "Select Primary Input" (0xCD) command will configure the two onboard relays to select the primary, legacy input. A "Select Auxiliary Input" (0xCF) command will configure the two onboard relays to select the auxiliary or secondary input. An "Enable Internal Link Analysis/Select PRN Generator Input" (0xCE) will configure the onboard relays to select the internal PRN generator as the input source, configure the PRN generator to operate with the same parameters (bit rate, PCM code, etc.) that the LS-040 D2 is currently set to, and enable the onboard PRN correlator to gather bit error information.

The LS-040 D2 may also be configured to perform bit error rate link analysis from external sources. If the LS-040 D2 is configured to select the primary or auxiliary input as PCM source, then sending an "Enable Link Analysis" (0xCA) command will enable the onboard PRN correlator, which will begin to gather bit error information on the incoming PCM stream. The LS-040 D2 can then be queried for status related to the bit error rate. Sending a "Disable Link Analysis" (0xC9) command will disable the PRN correlator without changing the input selected, with one exception. If the LS-040 D2 is in the "Enable Internal Link Analysis/Select PRN Generator Input" state, then sending the "Disable Link Analysis" (0xC9) command will select the primary input as well.

The default state upon power-up is to have the link analysis mode disabled, and the primary input selected. At any time during normal operations, the user can command the LS-040 D2 to internally select the PRN generator source as the input and perform an internal test of the LS-040 D2's operations. When this test is initiated, both external input sources are disconnected via an on-board relay and the PRN generator is selected as the source of the PCM stream.

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#### 4.2.6.5 *Disable/Enable Link Analysis Forced Error (0xCB and 0xCC)*

In order to more accurately assess an external PCM link. It is often desirable to determine if injected errors are being relayed through a system. The LS-040 D2 provides a means of forcing single-bit errors in the PRN stream provided by the on-board generator. A single bit error is injected in the output test stream when the “*Enable Link Analysis Forced Error*” command (0xCC) is issued. This mode can be disabled by issuing the “*Disable Link Analysis Forced Error*” command (0xCB)

The LS-040 D2's default state upon power-up is to have link analysis forced errors disabled.

#### 4.2.7 *Secondary PCM Decoder/Encoder Commands (0xD\_)*

The LS-040 D2 allows the user to program additional PCM input decoder and the PCM output encoder formats beyond those of command series 0xA\_ and 0xB\_. Since all 16 combinations are used for the primary PCM programming commands, an additional command set is required to provide these formats. Several of the inverted PCM formats are the same as others defined earlier (Inv. NRZ-M = NRZ-S). However, individual commands have been provided for user convenience. Table 4-8 describes the additional command sequences.

PCM Secondary Commands	Function
0xD0	Command PCM Input Decoder to RNRZ-17
0xD1	Command PCM Input Decoder to RNRZ-23
0xD2	Command PCM Input Decoder to Inv. NRZ-M
0xD3	Command PCM Input Decoder to Inv. NRZ-S
0xD4	Command PCM Input Decoder to Inv. BiΦ-M
0xD5	Command PCM Input Decoder to Inv. BiΦ-S
0xD6	Command PCM Input Decoder to Inv. DM-M
0xD7	Command PCM Input Decoder to Inv. DM-S
0xD8	Command PCM Input Decoder to Inv. Modified DM-M
0xD9	Command PCM Input Decoder to Inv. Modified DM-S
0xDA	Command PCM Input Decoder to Inv. RNRZ-11
0xDB	Command PCM Input Decoder to Inv. RNRZ-15
0xDC	Command PCM Input Decoder to Inv. RNRZ-17
0xDD	Command PCM Input Decoder to Inv. RNRZ-17
0xDE	Command PCM Output Encoder to RNRZ-17
0xDF	Command PCM Output Encoder to RNRZ-23

**Table 4-8** LS-040 D2 Secondary PCM Decoder/Encoder Commands

### 4.2.8 Status Commands (0xE\_)

The LS-040 D2 can provide operational and test status to the host processor via the parallel or serial bus interface. Table 4-9 Lists status commands and provides a reference paragraph for further response definitions.

Status Commands	Function	No. of Status Bytes	Reference Section	Reference Table
0xE0	Bit Sync Operational Status	3	4.2.8.1	4-10
0xE1	Link Analysis Update Status	3	4.2.8.2	4-11
0xE2	Link Analysis Bit Count Status	6	4.2.8.3	4-12
0xE3	Link Analysis Error Count Status	5	4.2.8.4	4-13
0xE4	Link Analysis Operational Status	5	4.2.8.5	4-14
0xE5	Estimated Es/No Status	11	4.2.8.6	4-15
0xE6	Estimated Signal Voltage Status	9	4.2.8.7	4-16
0xE7	Offset Frequency Status	9	4.2.8.8	4-17
0xE8	BIT Status	7	4.2.8.9	4-18
0xE9	Programmed PCM Bit Rate Status	10	4.2.8.10	4-19
0xEA	PCM Input Decoder Status	3	4.2.8.11	4-20
0xEB	PCM Output Encoder Status	3	4.2.8.12	4-21
0xEC	LBW Setting Status	3	4.2.8.13	4-22
0xED	Product Configuration Status	6	4.2.8.14	4-23
0xEE	Soft Bit Decision Percentages	10		
0xEF	EEPROM Value Read	6		

Table 4-9 LS-040 Status Commands

#### 4.2.8.1 Bit Sync Operational Status Response (0xE0)

The host can command the LS-040 D2 to send a status response which contains the state of the PLL lock, the input AGC threshold state, the BIT state and the Es/No state of the incoming PCM signal. If the host issues a "Bit Sync Operational Status" command (0xE0), the LS-040 D2 will respond with a three byte response message as defined in Table 4-10.

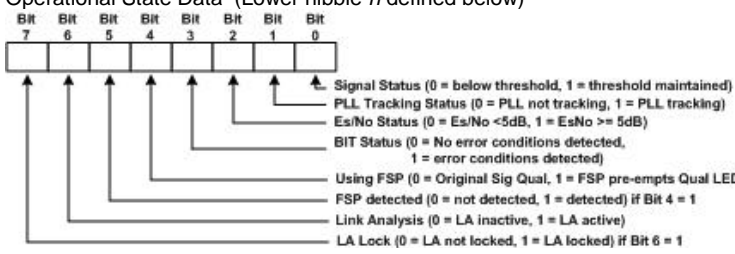
Status Byte	Status Value	Description	Applicable Values
1	0xE0	Status Command Echo	0xE0
2	0xFn	Terminal Address ( <i>n</i> = hex address of transmitting module)	0xF0 – 0xFF
3	0xnn	Operational State Data (Lower nibble <i>n</i> defined below)  <ul style="list-style-type: none"> <li>Signal Status (0 = below threshold, 1 = threshold maintained)</li> <li>PLL Tracking Status (0 = PLL not tracking, 1 = PLL tracking)</li> <li>Es/No Status (0 = Es/No &lt; 5dB, 1 = Es/No &gt;= 5dB)</li> <li>BIT Status (0 = No error conditions detected, 1 = error conditions detected)</li> <li>Using FSP (0 = Original Sig Qual, 1 = FSP pre-empt Qual LED)</li> <li>FSP detected (0 = not detected, 1 = detected) if Bit 4 = 1</li> <li>Link Analysis (0 = LA inactive, 1 = LA active)</li> <li>LA Lock (0 = LA not locked, 1 = LA locked) if Bit 6 = 1</li> </ul>	0x00- 0xFF

Table 4-10 Bit Sync Operational Status Definitions

### 4.2.8.2 Link Analysis Update Status Response (0xE1)

Prior to processing BER performance data, the host must verify that the correlator contents have been refreshed by the internal processing engine. The “Link Analysis Update Status” command (0xE1) will result in a three byte response from the LS-040 D2 as defined in Table 4-11.

Status Byte	Status Value	Description	Applicable Values
1	0xE1	Status Command Echo	0xE1
2	0xFn	Terminal Address (n = hex address of transmitting module)	0xF0 – 0xFF
3	0x3n	Bit Count/Error Count Update Status: 0x30 = Bit Count/Error Count not updated 0x31 = Bit Count/Error Count updated	0x30, 0x31

**Table 4-11** Link Analysis Update Status Definitions

### 4.2.8.3 Link Analysis Bit Count Status Response (0xE2)

The host may issue the “Link Analysis Bit Count Status” command (0xE2) at any time during normal operations to obtain the present bit count of the incoming PCM data. The LS-040 D2 will respond to this command with a six byte response as defined in Table 4-12.

Status Byte	Status Value	Description	Applicable Values
1	0xE2	Status Command Echo	0xE2
2	0xFn	Terminal Address (n = hex address of transmitting module)	0xF0 - 0xFF
3	0xnn	Bits 0-7 of the LS-040 D2 Bit Count	0x00 - 0xFF
4	0xnn	Bits 8-15 of the LS-040 D2 Bit Count	0x00 -0xFF
5	0xnn	Bits 16-23 of the LS-040 D2 Bit Count	0x00 - 0xFF
6	0x0n	Bits 24-25 of the LS-040 D2 Bit Count	0x00 - 0x03

**Table 4-12** Link Analysis Bit Count Status Definitions



**Note:** The “Link Analysis Bit Count Status” command can be issued at any time to get the present bit rate of the PCM stream. The link analysis functions do not have to be enabled for this data to be updated.

#### 4.2.8.4 Link Analysis Error Count Status Response (0xE3)

The host may issue the “Link Analysis Error Count Status” command (0xE3) at any time during link analysis operations to obtain the present bit error count of the incoming PCM data. The LS-040 D2 will respond to this command with a five byte response as defined in Table 4-13.

Status Byte	Status Value	Description	Applicable Values
1	0xE3	Status Command Echo	0xE3
2	0xFn	Terminal Address (n = hex address of transmitting module)	0xF0 - 0xFF
3	0xnn	Bits 0-7 of the LS-040 Error Count	0x00 - 0xFF
4	0xnn	Bits 8-15 of the LS-040 Error Count	0x00 - 0xFF
5	0xnn	Bits 16-19 of the LS-040 Error Count	0x00 - 0x0F

**Table 4-13** Link Analysis Error Count Status Definitions

#### 4.2.8.5 Link Analysis Operational Status Response (0xE4)

The host may issue the “Link Analysis Operational Status” command (0xE4) at any time during normal operations to obtain information on the state of the on-board PRN correlator. The LS-040 D2 will respond to this command with a five byte response as defined in Table 4-14.

Status Byte	Status Value	Description	Applicable Values
1	0xE4	Status Command Echo	0xE4
2	0xFn	Terminal Address (n = hex address of transmitting module)	0xF0 – 0xFF
3	0x3n	PRN correlator lock state: 0x30 = PRN correlator is locked 0x31 = PRN correlator is unlocked	0x30, 0x31
4	0x3n	PRN correlator history: 0x30 = PRN correlator lock maintained since last update 0x31 = PRN correlator unlocked since last update	0x30, 0x31
5	0x3n	Error Count Overflow: 0x30 = Error count overflow not detected 0x31 = Error count overflow detected	0x30, 0x31

**Table 4-14** Link Analysis Operational Status Definitions

#### 4.2.8.6 Estimated Es/No Status Response (0xE5)

The host may issue the “Estimated Es/No Status” command (0xE5) at any time during normal operations to obtain a calculated Es/No value from the DSP processing engine of the LS-040 D2. The LS-040 D2 will respond to this command with an eleven byte response as defined in Table 4-15. Status Byte 10 and 11 contain a value that represents the number of Frame Synchronization Patterns detected in the previous second. If Frame Sync Signal Quality is not allowed or if Frame Sync Signal Quality is not enabled, this value will be 0.



Status Byte	Status Value	Description	Applicable Values
1	0xE5	Status Command Echo	0xE5
2	0xF $n$	Terminal Address ( $n$ = hex address of transmitting module)	0xF0 – 0xFF
3	0x2 $n$	Es/No Level Sign Character (ASCII)	0x2B, 0x2D
4	0x3 $n$	Es/No Level 1's Value (ASCII)	0x30 – 0x39
5	0x2E	Es/No Level decimal point (ASCII)	0x2E
6	0x3 $n$	Es/No Level 1/10's Value (ASCII)	0x30 – 0x39
7	0x45	Es/No Level exponent character "E" (ASCII)	0x45
8	0x2 $n$	Es/No Level exponent sign character (ASCII)	0x2B, 0x2D
9	0x3 $n$	Es/No Level exponent value (ASCII)	0x30 - 0x39
10	0x $nn$	Most Significant Byte of FSP Frame Count	0x00 – 0xFF
11	0x $nn$	Least Significant Byte of FSP Frame Count	0x00 – 0xFF

**Table 4-15** Es/No Level Status Definitions

#### 4.2.8.7 Estimated Signal Voltage Status Response (0xE6)

The host may issue the “*Estimated Signal Voltage Status*” command (0xE6) at any time during normal operations to obtain an estimate from the coarse AGC circuitry of the input voltage level. The LS-040 D2 will respond to this command with a nine byte response as defined in Table 4-16.

Status Byte	Status Value	Description	Applicable Values
1	0xE6	Status Command Echo	0xE6
2	0xF $n$	Terminal Address ( $n$ = hex address of transmitting module)	0xF0 – 0xFF
3	0x2 $n$	Signal Level Sign Character (ASCII)	0x2B
4	0x3 $n$	Signal Level 1's Value (ASCII)	0x30 – 0x39
5	0x2E	Signal Level decimal point (ASCII)	0x2E
6	0x3 $n$	Signal Level 1/10's Value (ASCII)	0x30 – 0x39
7	0x45	Signal Level exponent character "E" (ASCII)	0x45
8	0x2 $n$	Signal Level exponent sign character (ASCII)	0x2B, 0x2D
9	0x3 $n$	Signal Level exponent value (ASCII)	0x30 - 0x39

**Table 4-16** Estimated Signal Voltage Level Status Definitions

#### 4.2.8.8 Offset Frequency Status Response (0xE7)

The host may issue the “*Offset Frequency Status*” command (0xE7) at any time during normal operations to obtain the offset tracking frequency of the LS-040 D2 symbol tracker. The LS-040 D2 will respond to this command with a nine byte response as defined in Table 4-17.

Status Byte	Status Value	Description	Applicable Values
1	0xE7	Status Command Echo	0xE7
2	0xFn	Terminal Address ( <i>n</i> = hex address of transmitting module)	0xF0 – 0xFF
3	0x2n	Offset Frequency Sign Character (ASCII)	0x2B, 0x2D
4	0x3n	Offset Frequency 1's Value (ASCII)	0x30 – 0x39
5	0x2E	Offset Frequency decimal point (ASCII)	0x2E
6	0x3n	Offset Frequency 1/10's Value (ASCII)	0x30 – 0x39
7	0x45	Offset Frequency exponent character "E" (ASCII)	0x45
8	0x2n	Offset Frequency exponent sign character (ASCII)	0x2B, 0x2D
9	0x3n	Offset Frequency exponent value (ASCII)	0x30 - 0x39

**Table 4-17** Offset Frequency Status Definitions

#### 4.2.8.9 BIT Status Response (0xE8)

The host may issue the “*BIT Status*” command (0xE8) at any time during normal operations. The LS-040 D2 continuously monitors power supplies and other critical internal systems for errors at power-up and during run-time operations. The LS-040 D2 will respond to this command with a seven byte response as defined in Table 4-18.

Status Byte	Status Value	Description	Applicable Values
1	0xE8	Status Command Echo	0xE8
2	0xFn	Terminal Address ( <i>n</i> = hex address of transmitting module)	0xF0 – 0xFF
3	0xnn	Overall BIT Status	0x00 – 0xFF
4	0xnn	Serial Interface Status	0x00 – 0xFF
5	0xnn	Functional Build Version Number	0x00 – 0xFF
6	0xnn	Synchronization and PCM generation status	0x00 – 0xFF
7	0xnn	Power monitoring status	0x00 – 0xFF

**Table 4-18** Built-In-Test (BIT) Status Definitions

#### 4.2.8.10 Programmed Bit Rate Status Response (0xE9)

The host may issue the “*Programmed Bit Rate Status*” command (0xE9) at any time during normal operations. This command may be useful in situations where the configuration EEPROM has been loaded on the board to retrieve previously programmed input rates for display. The LS-040 D2 will respond to this command with a ten byte response as defined in Table 4-19.

Status Byte	Status Value	Description	Applicable Values
1	0xE9	Status Command Echo	0xE9
2	0xFn	Terminal Address ( <i>n</i> = hex address of transmitting module)	0xF0 – 0xFF
3	0x9n	Bit Rate Setting x10Mbps	0x90-0x92
4	0x1n	Bit Rate Setting x 1Mbps	0x10-0x19
5	0x2n	Bit Rate Setting x 100Kbps	0x20-0x29
6	0x3n	Bit Rate Setting x 10Kbps	0x30-0x39
7	0x4n	Bit Rate Setting x 1Kbps	0x40-0x49
8	0x5n	Bit Rate Setting x 100bps	0x50-0x59
9	0x6n	Bit Rate Setting x 10bps	0x60-0x69
10	0x7n	Bit Rate Setting x 1bps	0x70-0x79

**Table 4-19** Programmed PCM Bit Rate Status Definitions

#### 4.2.8.11 PCM Input Decoder Status Response (0xEA)

The host may issue the “PCM Input Decoder Status” command (0xEA) at any time during normal operations. This command may be useful in situations where the configuration EEPROM has been loaded on the board to retrieve previously programmed PCM Decoder settings. The LS-040 D2 will respond to this command with a three byte response as defined in Table 4-20.

Status Byte	Status Value	Description	Applicable Values
1	0xEA	Status Command Echo	0xEA
2	0xFn	Terminal Address ( <i>n</i> = hex address of transmitting module)	0xF0 – 0xFF
3	0xnn	PCM Input Decoder Setting	0xA0-0xAF 0xD0-0xDD

**Table 4-20** PCM Input Decoder Status Definitions

#### 4.2.8.12 PCM Output Decoder Status Response (0xEB)

The host may issue the “PCM Output Decoder Status” command (0xEB) at any time during normal operations. This command may be useful in situations where the configuration EEPROM has been loaded on the board to retrieve previously programmed PCM Encoder settings. The LS-040 D2 will respond to this command with a three byte response as defined in Table 4-21.

Status Byte	Status Value	Description	Applicable Values
1	0xEB	Status Command Echo	0xEB
2	0xFn	Terminal Address ( <i>n</i> = hex address of transmitting module)	0xF0 – 0xFF
3	0xnn	PCM Output Encoder Setting	0xB0-0xBF 0xDE-0xDF

**Table 4-21** PCM Output Encoder Status Definitions

### 4.2.8.13 LBW Setting Status Response (0xEC)

The host may issue the “LBW Setting Status” command (0xEC) at any time during normal operations. This command may be useful in situations where the configuration EEPROM has been loaded on the board to retrieve the operational Loop Bandwidth settings. The LS-040 D2 will respond to this command with a three byte response as defined in Table 4-22.

Status Byte	Status Value	Description	Applicable Values
1	0xEC	Status Command Echo	0xEC
2	0xFn	Terminal Address ( <i>n</i> = hex address of transmitting module)	0xF0 – 0xFF
3	0xnn	Actual Loop Bandwidth Setting (see section 4.2.3)	0x81-0x8F

**Table 4-22** LBW Setting Status Definitions

### 4.2.8.14 Product Configuration Status Response (0xED)

The host may issue the “Product Configuration Status” command (0xED) at any time during normal operations. The response to this command provides operational and factory troubleshooting information. The LS-040 D2 will respond to this command with a three byte response as defined in Table 4-23.

Status Byte	Status Value	Description	Applicable Values
1	0xED	Status Command Echo	0xED
2	0xF0	Constant value of 0xF0	0xF0
3	0x3n	Product Configuration Identification: 0x31 = 10Mbps NRZ-L version D1 Emulation 0x32 = 20Mbps NRZ-L version D1 Emulation	0x31, 0x32
4	0xnn	On-board DSP Firmware Version (LSB)	0x00-0xFF
5	0xnn	On-board DSP Firmware Version (MSB)	0x00-0xFF
6	0xnn	FPGA Firmware Revision Number	0x00-0xFF

**Table 4-23** Product Configuration Status Definitions for Parallel Port ID = 0x31 or 0x32

Status Byte	Status Value	Description	Applicable Values
1	0xED	Status Command Echo	0xED
2	0xFn	On-board FPGA Firmware Version	0xF0 – 0xFF
3	0x3n	Product Configuration Identification: 0x41 = 10 Mbps NRZ-L version 0x42 = 20 Mbps NRZ-L version (25 Mbps requires factory installed hardware filters)	0x41, 0x42
4	0xnn	On-board DSP Firmware Version (MSB)	0x00-0xFF
5	0xnn	On-board DSP Firmware Version middle byte	0x00-0xFF
6	0xnn	On-board DSP Firmware Version (LSB)	0x00-0xFF

**Table 4-24** Product Configuration Status Definitions for Parallel Port ID = 0x41 or 0x42

#### 4.2.8.15 Soft Bit Decision Percentages (0xEE)

Status Byte	Status Value	Description	Applicable Values
1	0xEE	Status Command Echo	0x00 – 0x64
2	0x08	Number of bytes to follow (always 8)	0x00 – 0x64
3	0xnn	Definite 0's Percentage	0x00 – 0x64
4	0xnn	Strong 0's Percentage	0x00 – 0x64
5	0xnn	Probable 0's Percentage	0x00 – 0x64
6	0xnn	Weak 0's Percentage	0x00 – 0x64
7	0xnn	Definite 1's Percentage	0x00 – 0x64
8	0xnn	Strong 1's Percentage	0x00 – 0x64
9	0xnn	Probable 1's Percentage	0x00 – 0x64
10	0xnn	Weak 1's Percentage	0x00 – 0x64

Table 4-25 LS-040 D2 Soft Bit Percentages

#### 4.2.8.16 EEPROM Read Value (0xEF)

The host can perform a read of the on-board EEPROM chip. The EEPROM is arranged into 16 pages of 64 two byte words called lines. A request for to read a value from the EEPROM consists of the 0xEF byte followed by the page number in a byte (0 – 15), followed by the line number (0 – 63), followed by the 0x0A Master Configuration Command. The LS-040 D2 will return as a status response six bytes.

Status Byte	Status Value	Description	Applicable Values
1	0xEF	Status Command Echo	0xED
2	0x04	Number of bytes to follow (always 4)	0x04
3	0x3n	The Page number of the value requested (0 – 15)	0x00 – 0x0F
4	0xnn	The Line number of the value requested (0 – 63)	0x00 – 0x3F
5	0xnn	The Most Significant Byte of the value requested	0x00 – 0xFF
6	0xnn	The Least Significant Byte of the value requested	0x00 – 0xFF