LS-40-B

Drive Bay Bit Synchronizer

Hardware User's Manual

Document:	U40B0101
Editor:	D. Spielman
Date:	6/19/2008
Release:	Initial

Lumistar, Inc.

5870 El Camino Real

Carlsbad, California 92008

(760) 431-2181

www.lumi-star.com

Lumistar,Inc.
5870 El Camion Real
Carlsbad, CA 92008
(760) 431-2181
(760) 431-2665 Fax
www.lumi-star.com

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 Introduction

1.1 General

This user's manual for the Lumistar LS-40-B drive bay programmable digital PCM bit synchronizer is intended to provide physical, functional, and operational information for the end user. The LS-40-B drive bay bit synchronizer utilizes the same technology found in the popular Lumistar LS-40-DB daughterboard bit sync and the all-digital design assures a consistent product with high reliability and long-term stability.

By essentially packaging the LS-40-DB into a stand alone PC drive bay housing, the LS-40-B offers the same Built-In Test features of both *Auto-Test* upon start up and *Command-Test* allowing the user to manually check the bit synchronizer functions at any time. The bit synchronizer includes a data correlator for reading pseudo-random test patterns, as well as frame sync words. With the built-in BER reader, the user has the ability to generate internal pseudo-random patterns and calculate internal bit error rates (BER) with or without the injection of forced errors. Various status indicators are also available to the user through the included software.

As its primary function, the LS-40-B drive bay bit synchronizer provides correlated clock and data recovery from an incoming PCM stream. The LS-40-B can translate various PCM formats and provides a user programmable PCM output format useful for tape storage or as a means of providing PCM format translation. The LS-40-B can be programmed to support data rates from 50 bps to 20 Mbps for NRZ PCM codes and 50 bps to 10 Mbps for all other support self-clocking PCM codes.

Table 1-1 on page 8 provides the specifications for electrical, mechanical, and operational characteristics of the LS-40-B drive bay bit synchronizer. A block diagram of the LS-40-B is shown in Figure 1-1 on page 9.

1.2 Manual Format and Conventions

This manual contains the following sections:

- Chapter 1 provides a brief product overview and technical specifications
- Chapter 2 provides a theory of operation for the LS-40-B
- Chapter 3 provides installation and configuration instructions
- Chapter 4 provides an introduction to the stand-alone Windows control software
- Chapter 5 provides programming information

Throughout this document, several document flags will be utilized to emphasis warnings or other important data. These flags come in three different formats: Warnings, Cautions, and Information. Examples of these flags appear below.

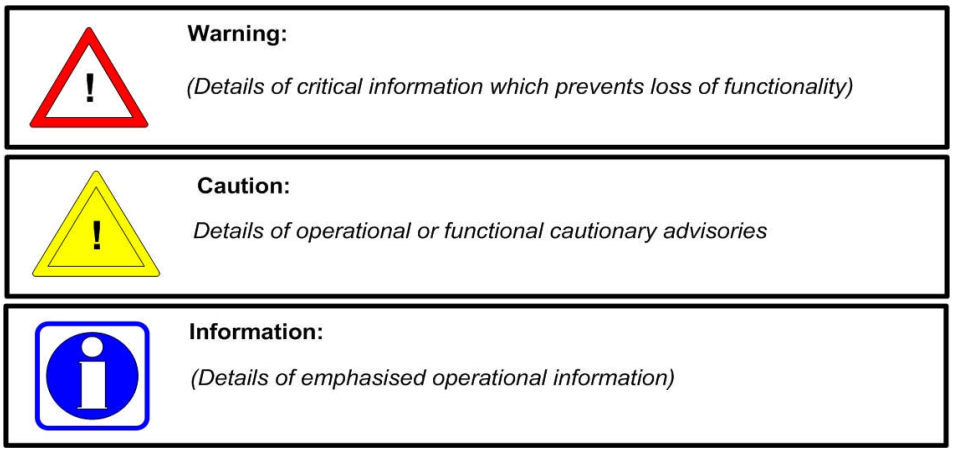


Table 1-1 Specifications for the LS-40-B Bit Synchronizer		
Category:	**Specifications:**	**Details:**
Mechanical		
	Envelope Dimensions	5.785"(L) x 4.0"(W) x 0.55" (H)
	Form Factor	Basic Desktop Hard-drive footprint
	Weight	< 5oz.
Electrical		
	Individual power requirements	+5VDC @ 850mA
		+12VDC @ 10.7mA
	Total Power	< 6.9W
Inputs		
	Quantity	1 SE/Differential Input; Jumper Selected
	Impedance	50, 75 or 1K Ω; Jumper Selectable
	Rates (Option dependent)	50-20Mbps NRZ Codes; 50-10Mbps others
	Polarity	Normal or Inverse; Software Programmable
	Signal Amplitude	0.5V to 10V p-p
	Maximum Voltage permissible	25V RMS
	Loop Bandwidth (LBW) settings	0.01 to 2% (data rate dependent)
	Acquisition Range	+/- (4 x LBW Setting)
	Tracking Range	+/- (10 x LBW Setting)
	Mean Acquisition Time	100-150 bits
Outputs		
	NRZ-L Data Output	+TTL, -TTL
	0^o Clock Output	+TTL, -TTL
	PCM Output	1V p-p @ 50 @; Programmable Line Codes
	PCM PRN Output	+TTL, -TTL; Programmable Line Codes
	PCM PRN Patterns	2^{11}-1, 2^{15}-1; Programmable
Control/Status		
	Serial Control/Status Interface	RS-232C Interface; Selectable BAUD rate
PCM Line Codes		
	Non-return to Zero Codes	NRZ-L, NRZ-M, NRZ-S
	Bi-Phase Codes	BiΦ-L, BiΦ-M BiΦ-S
	Delay Modulation (Miller) Codes	DM-M, DM-S, M^2M, M^2S
	Return to Zero Codes	RZ
	Randomized Codes	RNRZ-L, RNRZ-S, RNRZ-M
	Randomizing Sequences	2^{11}-1, 2^{15}-1, 2^{17}-1, 2^{23}-1
Environmental		
	Temperature, Operational	0^o to 70^o C (Commercial)
	Temperature, Storage	-20^o to 70^o C
	Humidity, non-condensing	$<40^o$ C 0-90%, $>40^o$ C 0 to 75%

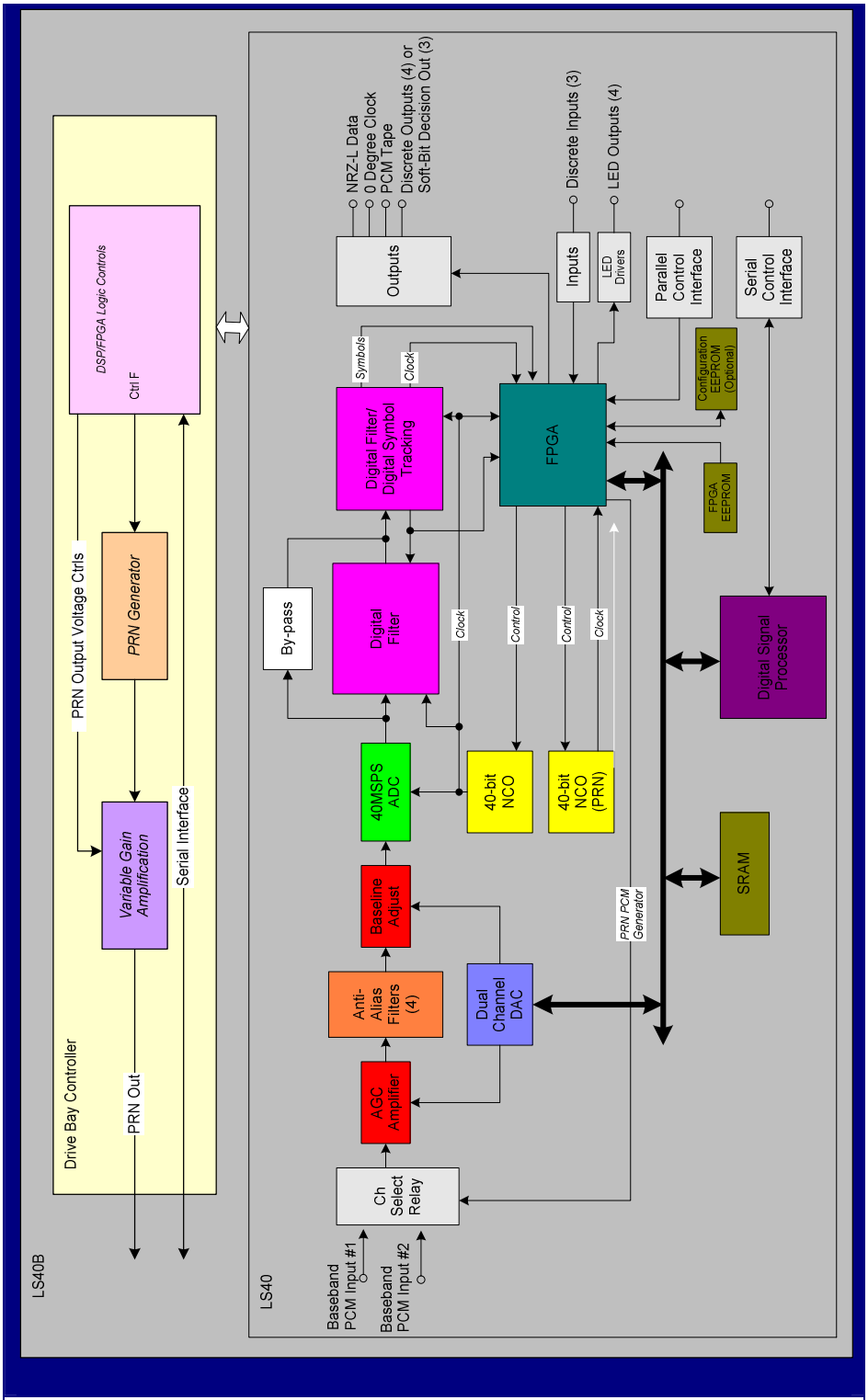


Figure 1-1 Block Diagram of the LS-40-B Bit Synchronizer

2 Theory of Operation

In order to more clearly understand the operation of the LS-40-B drive bay bit synchronizer, the generic functionality all bit synchronizers needs to be discussed. The primary functions of any bit synchronizer are as follows:

- Receive an *analog* Pulse Code Modulated (PCM) input data stream
- Adjust the incoming data stream for various signal levels and offsets
- Filter unwanted frequencies and noise from the primary bands of interest
- Process the data stream to recover the incoming data with a correlated clock
- Provide the correlated clock and data output for further data processing and/or data storage

Utilizing various Digital Signal Processing (DSP) technologies, the LS-40-B provides all of these functions. This digital architecture provides for greater signal integrity and control and reduces temperature sensitivity while at the same time utilizing far less power than a traditional analog bit synchronizer. Because the LS-40-B contains no analog data filters, any variations in performance from one unit to the next are nearly eliminated.

2.1 Input Section

As shown in Figure 1-1 on page 9, the input section of the LS-40-B drive bay bit synchronizer is composed of the following elements:

- Self-test & input section relay
- Input termination impedance selection
- Digital feed-back Automatic Gain Control (AGC) circuitry
- Four (4) fixed anti-alias filters
- Digital feed-back baseline restoration adjustment circuit

The self-test and input selection relay is used in conjunction with the Built-In-Test (BIT) provisions of the LS-40-B to provide switching of the on-board PRN generator test signal to the input section for power-up functional tests. The relay also provides user selection of the multiple PCM input signals. For more on this relay see section 2.4 on page 12.

To match the output impedance of the PCM source, multiple input terminations are provided. Three termination impedances are supported: 50Ω ohms, 75Ω ohms, and 1KΩ. In addition to these typical impedances, custom impedances are also available. Please consult the factory for availability.

The AGC amplifier adjusts the input signal to the proper levels for processing. Nominally, the input signal level may vary between 500mVp-p and 10Vp-p. The maximum input signal level permissible without damage is 25V p-p. A 10-bit Digital-to-Analog Converter (DAC) controls the AGC circuit, with data being fed to the DAC via

the DSP engine. The DSP engine constantly monitors the incoming signal for variations in amplitude and adjusts the signal level accordingly.

Following the AGC amplifier, the signal passes through a bank of one of four anti-alias filters. These fixed frequency low pass filters are used to eliminate the high frequency interfering signals produced within the LS-40-B. The high frequency interferers include the digital decimation and interpolation employed by the DSP engine. The filters block these unwanted by-products and prevent them from interfering with the input signal. Without the filtering, these digital "disturbers" would fall within the bands of interest.

A digitally controlled baseline restoration circuit forms the final stage of the input section. The incoming PCM signal may be either DC or AC coupled. When AC coupled, the front end of the LS-40-B blocks the DC component of the incoming signal and passes the AC component. However, slight variations due to; "baseline gallop[1]" may still interfere with the proper processing of the PCM signal. To compensate for this, the DSP engine feeds digital correction factors back to the baseline restoration circuit.

2.2 Digital Filtering and Processing

After the input PCM signal has been gain & baseline compensated in the front end, it is digitize by a high-performance Analog-to-Digital Converter (ADC). The resulting digital data is sent through a series of decimation/interpolation filtering elements followed by a symbol tracker. Symbol and clock information is further processed by a Field Programmable Gate Array (FPGA). The FPGA converts and decodes the input PCM into the desired format.

Two individually controlled, 40-bit NCOs (Numerical Controlled Oscillators) provide the clocks used by the processing engine and the PRN test generator. The two NCOs use a common precision crystal oscillator as a reference source to minimize the overall jitter and drift of the clock.

2.3 Control, Sequencing and Memory

At the core of the LS-40-B architecture is a 30 million-instruction-per-second DSP and a 400,000 gate FPGA. The FPGA provides the hardware control logic for the bit sync while the dedicated processor is used for overall software control and sequencing of the DSP engine. The processor also provides direction and control of the user interface, as well as interfacing to components of the system memory.

The memory elements on the LS-40-B include the following: 1) SRAM, 2) Internal DSP FLASH memory, 3) FPGA configuration EEPROM, and 4) Serial configuration

[1] In the phenomenon known as *baseline gallop*, the DC level of a signal slowly rises and then falls with time. This can adversely affect the performance of some bit synchronizer designs, so it's important to eliminate this condition whenever possible.

EEPROM. The processor stores the executable code in its internal FLASH memory, which is non-volatile and is **not** accessible to the user. This memory is not programmed during normal use and contains no storage of operational parameters. The SRAM is used for data variable storage. This memory is volatile and is cleared upon loss of power. The FPGA is loaded at power-up via a serial EEPROM, which is non-volatile and is **not** accessible to the user. The LS-40-B contains a serial EEPROM that (optionally) stores information about the last valid configuration of the bit sync. This includes parameters such as bit rates, PCM processing codes, loop-bandwidth settings, etc. This memory is non-volatile and will be automatically configured by the user during setup of the bit sync, if the option to retain this information is chosen. This option is set at the factory to not allow the EEPROM to store any configuration data.

2.4 User Control and Status Interfaces

The LS-40-B is controlled via one of two standard RS/EIA serial interface methods: RS/EIA-232 or EIA/RS-485. The unit it shipped from the factory configured for control via an RS-232 interface.

2.4.1 RS-232 Interface Mode

The RS-232 interface is the factory configured default. This interface is capable of being run at rates between 9.6k BAUD and 115.2k BAUD with a default rate of 57.6k BAUD. In order for this interface method to be active, the configuration switches of SW1 have to be set as indicated: SW1-1 through SW1-4 switched to the OFF position.

If SW1-5 is switched to the ON position, the module address switches are ignored and the unit is set to utilize the RS-232 interface at 57.6k BAUD.

2.4.2 RS-485 Interface Method (Future)

Details of this interface method will be provided in future firmware releases.

2.5 PCM Link Analysis Functions

The LS-40-B provides a Link Analysis function. When enabled, this feature outputs a PRN pattern that can be looped internally to test the LS-40-B, or externally to test an exterior PCM processing loop. The PCM output can be programmed to be any of the supported LS-40-B line formats[2]. The PRN pattern generator can be programmed for a pseudo-random pattern length of 2^{11}-1 (2,047 bits) or 2^{15}-1 (32,767) bits.

When using the LS-40-B Link-analysis function to stimulate an external PCM processing path, the returned PCM stream is connected to the LS-40-B where a sliding-correlator is used to count Bit Errors and calculate Bit Error Rate (BER) performance of the external

[2] See Table 1-1 on page 8 for specific PCM line codes.

PCM link. This function is useful in determining link integrity and overall performance. Figure 2-1 below shows the interconnection of this test setup.

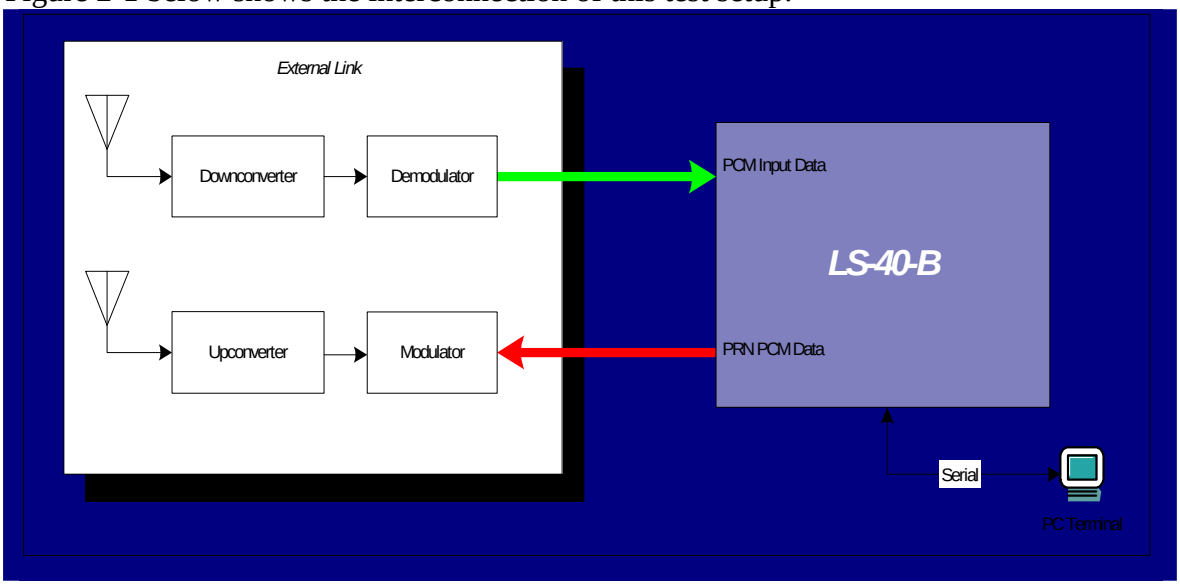


Figure 2-1 PCM Link Analysis using the LS-40-B Drive Bay Bit Synchronizer

3 Installation and Configuration

Chapter 3 provides installation and configuration information for the LS-40-B drive bay bit synchronizer. This chapter will familiarize the user with the layout of the module, and provide information on the proper installation and interconnection of the hardware.

3.1 Product Outline Diagram

Figure 3-1 on page 15 contains an outline diagram of the top and front views of the LS-40-B drive bay enclosure. Connector locations and switch positions are indicated.

3.2 Hardware Configuration

The LS-40-B bit sync design contains configuration switches to control various functions. Figure 3-2 on page 16 contains a diagram of the configuration switches along with the default factory positions for these switches.

3.3 Physical Installation

To install the LS-40-B in the target computer system, follow the procedure presented below.

1. Perform a normal system shutdown of the PC system and remove the primary power plug from the computer.
2. Set the configuration switches (SW1) based on the required user configuration. See Figure 3-2 on page 16 for a description of each switch and their functions. Use the following information to guide in configuration setups:
   - The first four switch positions are used to set one of 15 available RS-485 multi-drop module addresses. If the address is set to 0 (SW1-1 through SW1-4 off), then the RS-232 interface mode is automatically activated.
   - If SW1-5 is placed in the ON position, then the module defaults to RS-232 operation at 57.6K BAUD. This switch position overrides the state of SW1-1 through SW1-4.
   - SW1-6 is reserved for future use and should remain in the OFF position.
   - SW1-7 is used to terminate the serial interface bus when the RS-485 serial mode is utilized. This switch should be used to maintain signal integrity for long line lengths and should only be switched to the ON position on the last module on the physical bus. This switch should remain in the OFF position when the RS-232 serial mode is being utilized.
   - SW1-8 is a factory use switch and should remain in the OFF position at all times for normal bit sync operation.
3. Install the LS-40-B in and unobstructed hard-drive bay using the screws supplied. Ensure that the installation provides room for the I/O connections.
4. Ensure that sufficient cooling air is circulated around the package. This will prevent long-term heat related damage to this bit sync.

5. Connect the serial control/IO interface to an RS-232/RS-485 interface as defined by the user requirements.
6. Using the provided software installation CD, execute the *Ls40BSetup.exe* installation script.

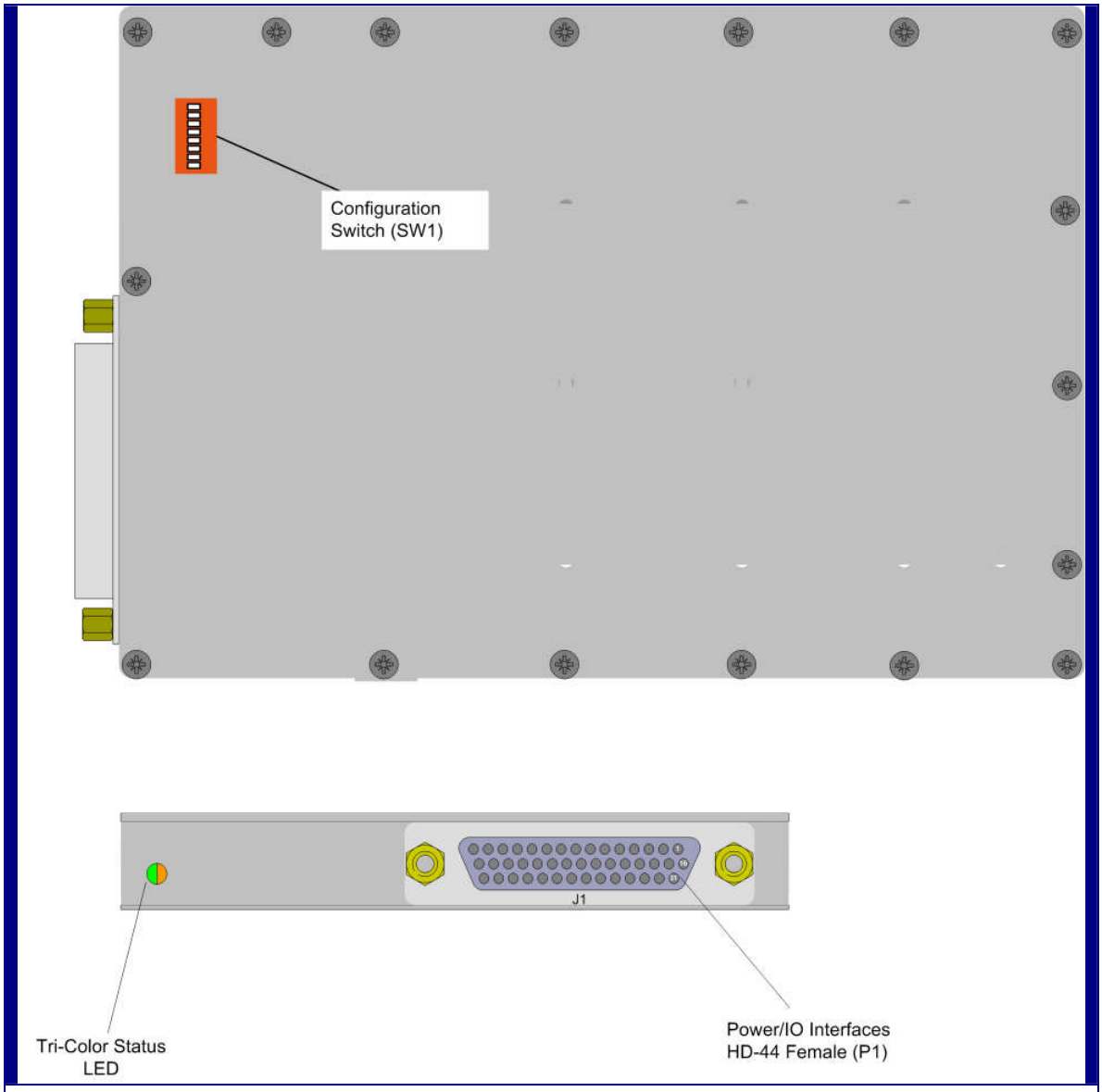


Figure 3-1 LS-40-B Mechanical Outline Drawing

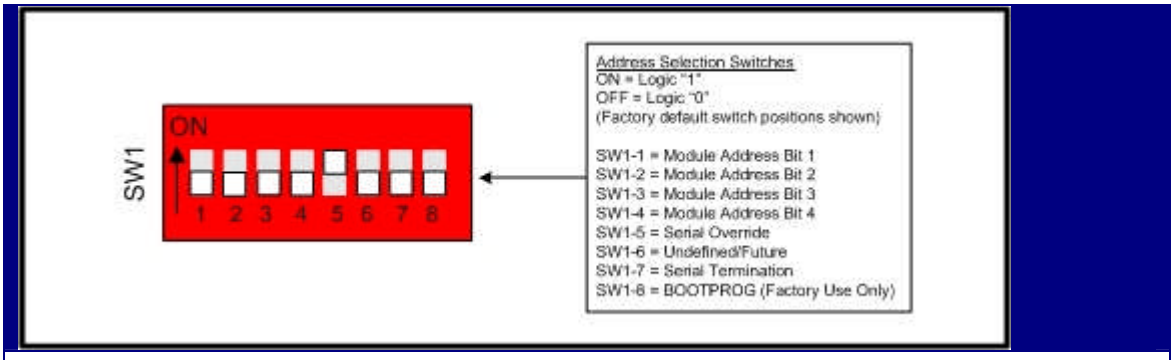
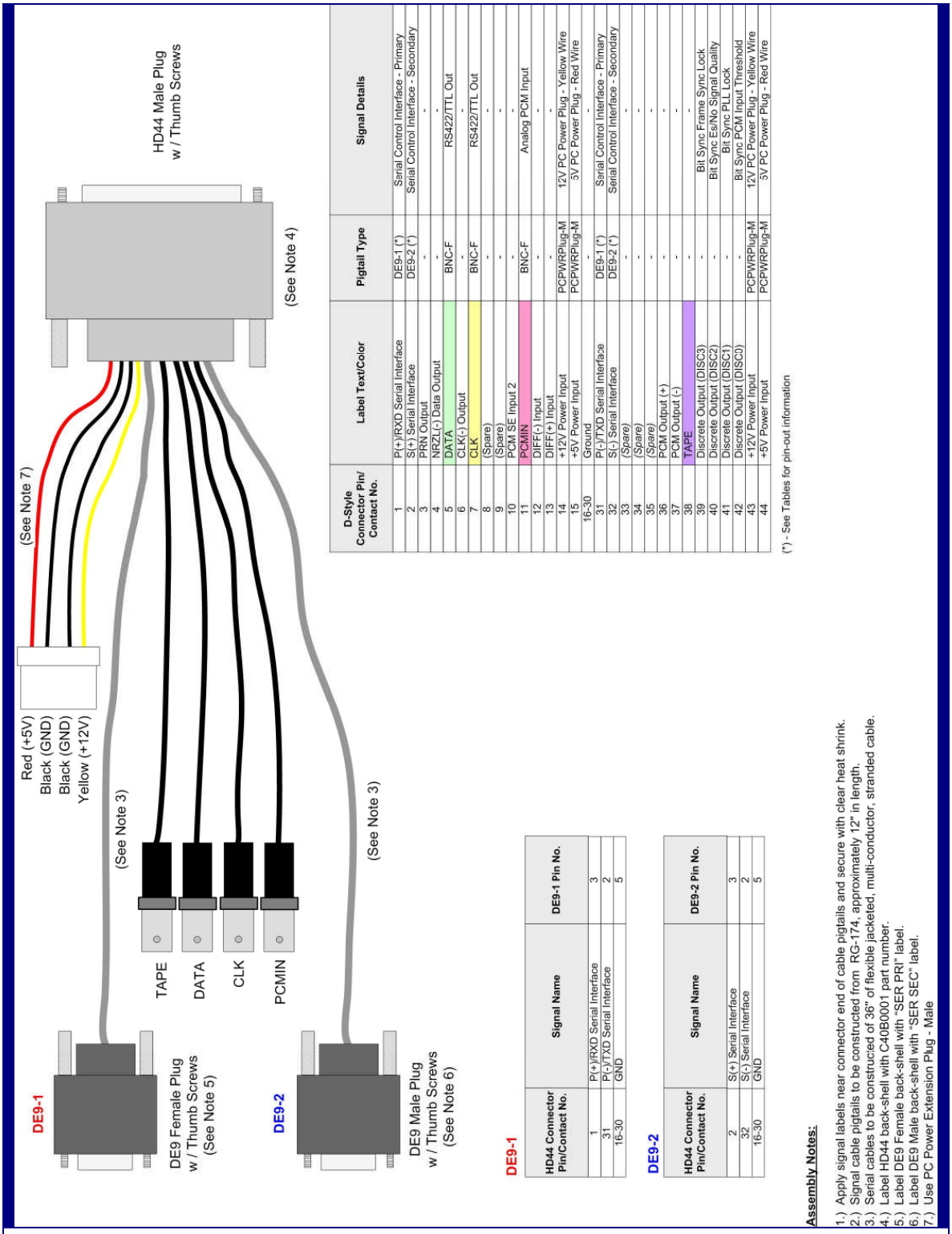


Figure 3-2 Drive Bay Bit Sync Configuration Switch Settings

3.4 Interconnection

As shown in Figure 3-3 below, the LS-40-B drive bay bit synchronizer is shipped with a mating pigtail cable to interface with the J1 connector. Figure 3-4 on page 17 illustrates this cable and its signals.

Figure 3-3 LS-40-B With Supplied Pigtail Connector



D-Style Connector Pin/ Contact No.	Label Text/Color	Pigtail Type	Signal Details
1	P(+)/RXD Serial Interface	DE9-1 (*)	Serial Control Interface - Primary
2	S(+) Serial Interface	DE9-2 (*)	Serial Control Interface - Secondary
3	PRN Output	-	-
4	NRZL(-) Data Output	-	-
5	DATA	BNC-F	RS422/TTL Out
6	CLK(-) Output	-	-
7	CLK	BNC-F	RS422/TTL Out
8	(Spare)	-	-
9	(Spare)	-	-
10	PCM SE Input 2	-	-
11	PCMIN	BNC-F	Analog PCM Input
12	DIFF(-) Input	-	-
13	DIFF(+) Input	-	-
14	+12V Power Input	PCPWRPlug-M	12V PC Power Plug - Yellow Wire
15	+5V Power Input	PCPWRPlug-M	5V PC Power Plug - Red Wire
16-30	Ground	-	-
31	P(-)/TXD Serial Interface	DE9-1 (*)	Serial Control Interface - Primary
32	S(-) Serial Interface	DE9-2 (*)	Serial Control Interface - Secondary
33	(Spare)	-	-
34	(Spare)	-	-
35	(Spare)	-	-
36	PCM Output (+)	-	-
37	PCM Output (-)	-	-
38	TAPE	-	-
39	Discrete Output (DISC3)	-	Bit Sync Frame Sync Lock
40	Discrete Output (DISC2)	-	Bit Sync Es/No Signal Quality
41	Discrete Output (DISC1)	-	Bit Sync PLL Lock
42	Discrete Output (DISC0)	-	Bit Sync PCM Input Threshold
43	+12V Power Input	PCPWRPlug-M	12V PC Power Plug - Yellow Wire
44	+5V Power Input	PCPWRPlug-M	5V PC Power Plug - Red Wire

(*) - See Tables for pin-out information

DE9-1

HD44 Connector Pin/Contact No.	Signal Name	DE9-1 Pin No.
1	P(+)/RXD Serial Interface	3
31	P(-)/TXD Serial Interface	2
16-30	GND	5

DE9-2

HD44 Connector Pin/Contact No.	Signal Name	DE9-2 Pin No.
2	S(+) Serial Interface	3
32	S(-) Serial Interface	2
16-30	GND	5

Assembly Notes:

1.) Apply signal labels near connector end of cable pigtails and secure with clear heat shrink.
2.) Signal cable pigtails to be constructed from RG-174, approximately 12" in length.
3.) Serial cables to be constructed of 36" of flexible jacketed, multi-conductor, stranded cable.
4.) Label HD44 back-shell with C40B0001 part number.
5.) Label DE9 Female back-shell with "SER PRI" label.
6.) Label DE9 Male back-shell with "SER SEC" label.
7.) Use PC Power Extension Plug - Male

Figure 3-4 LS-40-B Pigtail Connectors

4 Using the LS-40-B with the Standalone Windows Control Program

The LS-40-B is configured with a Microsoft Windows application for control and setup of the bit sync hardware. The LS-40-B software consists of a simple primary setup window, shown in Figure 4-1 below, and several specific function setup windows that will be described in this chapter.

Figure 4-1 LS-40-B Primary Setup Window

The primary setup window has three top-level commands that inclue: ***Config***, ***Setup***, and ***About***. Each will be described in subsequent paragraphs.

The ***Config***uration command deals with the setup of the serial communication path between the LS-40-B and the host computer. Invoking the command produces the setup window shown below left in Figure 4-2. By placing the mouse cursor within the "***Com Settings***" box and right clicking, the user may specify the number of LS-40-B's units to be controlled from the application (up to four) by selecting the *Number of Cards*[3] command from the menu. The user may also configure the individual serial communications parameters for each LS-40-B by selecting the tab associated with the unit, right clicking the mouse cursor, and selecting the *Com Settings* command from the menu. The resulting setup screen is shown below right in Figure 4-2.

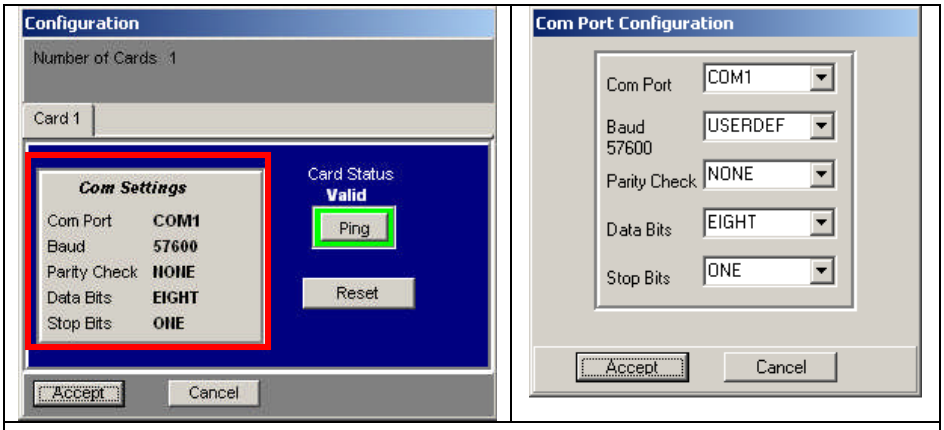
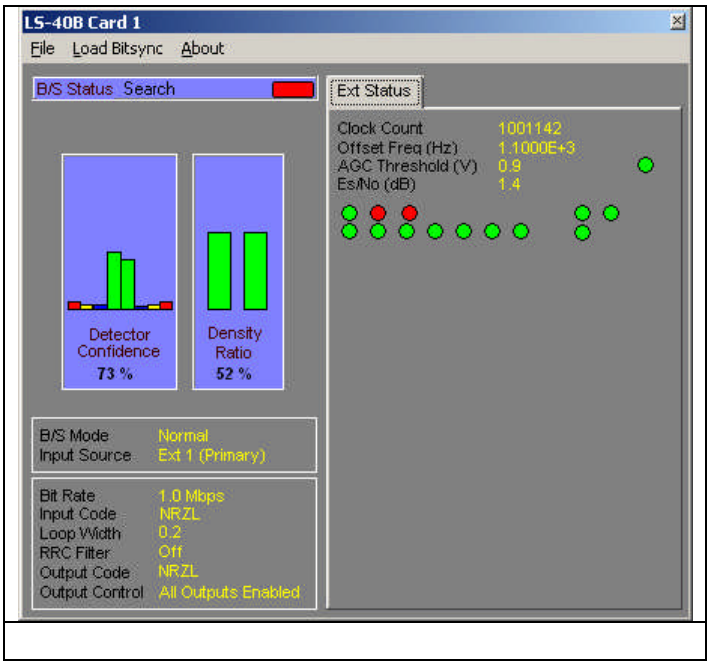


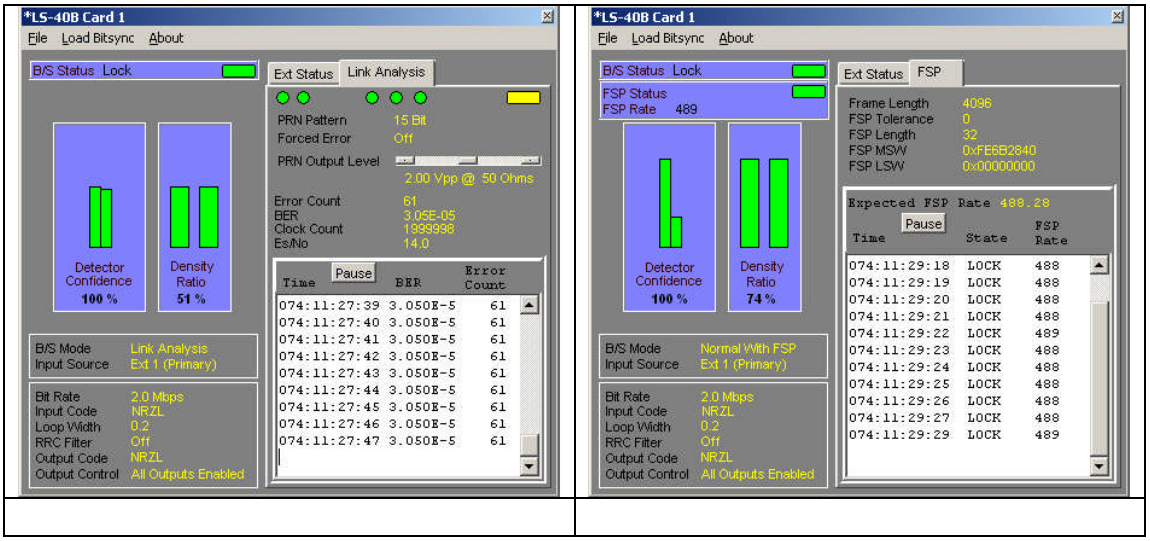
Figure 4-2 LS-40-B Serial Communications Setup Windows

The *Con Port Configuration* window allows the user to select the com port number (1 to 16), the Baud Rate (up to 256 K), the Parity (None, Odd, Even, Mark, or Space), the word length (5, 6, 7, or 8), and the number of stop bits (one, one and a half, or two).

[3] In this case, the word, "cards" actually refers to the number of LS-40-B units connected to the host computer.



Bit Sync Mode



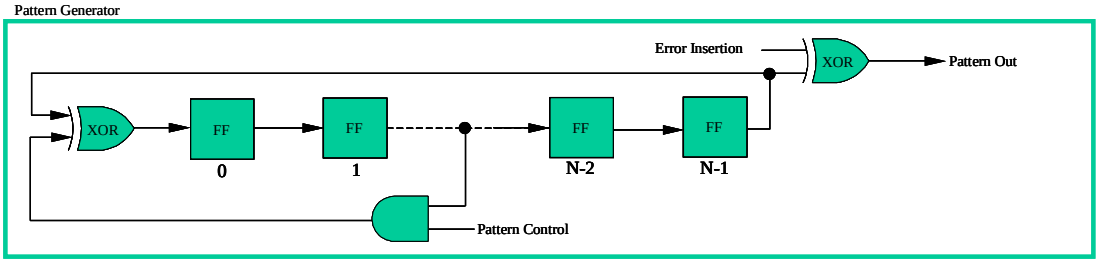
Link Analysis Mode

The BERT is an instrument that generates a special digital test signal. This signal is sent through the system and the BERT counts the number of bit errors in the recovered signal and provides the user with a Bit Error Rate, or BER. The BER measurement is one of the

fundamental parameters that characterize the overall performance of the telemetry system and of many of its components.

A "Geek" Technical Tidbit:

The basic performance measure of any digital transmission system, of which a telemetry system is an example, is the probability that any transmitted bit will be received in error. These bit errors when they occur can be introduced in many places along the path the signal flows through. Errors introduced into the transmission are often random in nature and are strongly affected by system parameters such as *signal level*, *noise level*, and *timing jitter*.



The actual digital test signal generated by the BERT employs a Pseudorandom Noise (PN) sequence to simulate traffic and to examine the transmission system for pattern-dependent tendencies or critical timing effects. An example of such a PN generator is shown above. Selecting the proper PN sequence that will be appropriate for the particular system being tested is important. Some of the key properties of the selected PN sequence that are of importance include: 1) The length of the PN Sequence. 2) The Linear Feedback Shift Register configuration used to implement the PN generator (this defines the binary run properties of the sequence). 3) Spectral line spacing of the sequence (which depends on the bit rate of the sequence). Although there are many, two PN sequence patterns have been standardized by the CCITT[4] for testing digital transmission systems. They are based on 15-stage and 23-stage Linear Feedback Shift Register configurations.

As mentioned earlier, errors introduced into the transmission of a digital signal are often random in nature and are strongly affected by system parameters such as signal level, noise level and noise bandwidth, timing jitter, and data rate. The BER is actually a probability and is related to another system parameter - E_b/N_0 (pronounced ebbno). E_b/N_0 is the ratio of the energy-per-bit and the noise-power-per-unit-bandwidth of the digital transmission. The E_b/N_0 as a quantity is a theoretical convenience rather than the direct output of a test measurement device. The parameters that do in effect define the E_b/N_0, and that can be directly measured by the user are the received carrier power (C), and the received noise power (N). These measured parameters, in addition to the noise bandwidth

[4] CCITT Rec. 0151, Yellow Book, Vol. 4 Fascicle IV.4 Recommendation 0.151.

(W) of the system component being tested and the data rate (R_b) of the signal define the system E_b/N_0 in the following relationship:

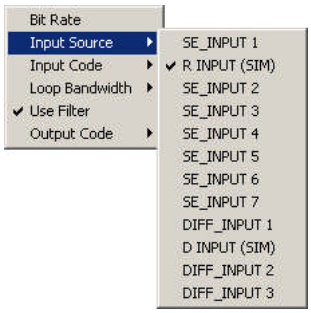
$$\frac{Eb}{No} = \left(\frac{C}{N}\right)\left(\frac{W}{Rb}\right)$$

With the system E_b/N_0 defined in terms of measurable quantities, we can now define the BER probability. For example, the BER probability of a digital signal employing bipolar signaling expressed in terms of E_b/N_0 has the following relationship:

$$Pe = Q\left(\sqrt{\frac{2Eb}{No}}\right)$$

Where E_b is the average energy of a modulated bit, and N_0 is the noise power spectral density (noise in 1-Hz bandwidth). The value Q(X) is called the Gaussian Integral Function and is usually calculated numerically. Note, the quantity "X" will vary mathematically for each type of modulation and signal encoding used in the system.

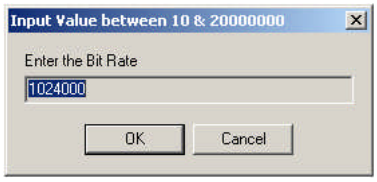
Input Source



The LS-40-B Bit Synchronizer can support up to twelve (12) separate input signals. The inputs include both single-ended (SE) and differential (D/Diff) with 50Ω, 75Ω, or 1KΩ (Jumper Select) input impedance. The input signal amplitude supported ranges from 0.1 V pp to 10 V pp. To select the appropriate input, invoke the **Input Source** command and select the specific input from the drop-down list.

Input Bit Rate

The LS-40-B Bit Synchronizer can operate over an input range of 100 bits per second to 20 Mbps for all NRZ codes, or from 100 bits per second to 10 Mbps for the Bi-Phase and Miller codes. By invoking the **Input Bit Rate** command, the user may enter the required input data rate in bits per second.



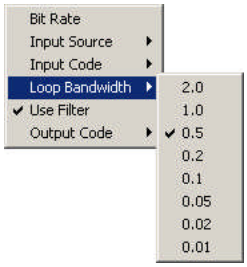
Input Code

The LS-40-B Bit Synchronizer supports the PCM input code types specified in Table 4-1 below. Both normal and inverted variants are available. To select the appropriate input code, invoke the **Input Code** command and select the specific input code from the drop-down list.

Table 4-1 LS-40-DB Supported PCM Input Codes (normal or inverted)	
NRZ codes	NRZ-L, NRZ-M, NRZ-S
RZ codes	RZ
Split phase codes	BiPhase-L, BiPhase-M, BiPhase-S
Miller codes	DM-M, DM-S, M^2-M, M^2-S
Randomized codes	RNRZ-L, RNRZ-M, RNRZ-S
Randomization sequence	2^{11}-1, 2^{15}-1, 2^{17}-1, 2^{23}-1 (normal or inverted)

Loop Bandwidth

The Loop-Bandwidth of the PLL circuit in the LS-40-B may be programmed by the user from 0.01% to 2% depending on the bit rate of the input signal. As described in the "Technical Tidbit" above, The Acquisition Range (0.04% to 8%, depending on the Loop-Bandwidth selected) and the Tracking Range (0.1% to 20%, again depending on the Loop-Bandwidth selected) are both heavily dependent on the loop bandwidth of the PLL. To select the appropriate loop bandwidth, invoke the **Loop Bandwidth** command and select the specific value from the drop-down list



Use Filter

The user may enable additional data filtering, prior to the actual phase lock loop of the bit synchronizer by invoking the **Use Filter** command. The additional filter uses a "Raised-Root Cosine" topology and is used to improve the performance metric of the bit synchronizer.

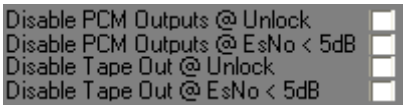
Output Code

The LS-40-B Bit Synchronizer supports the PCM output code types specified in Table 4-2 below. Both normal and inverted variants are available. To select the appropriate output code, invoke the **Output Code** command and select the specific output from the drop-down list.

Table 4-2 LS-40-DB Supported PCM Output Codes	
NRZ codes	NRZ-L, NRZ-M, NRZ-S, INV_NRZL
RZ codes	RZ, INV_RZ
Split phase codes	BiPhase-L, BiPhase-M, BiPhase-S, INV_BIOL
Miller codes	DM-M, DM-S, M^2-M, M^2-S
Randomized codes	RNRZ-L, RNRZ-M, RNRZ-S
Randomization sequence	2^{11}-1, 2^{15}-1, 2^{17}-1, 2^{23}-1

Quick React Mode

The LS-40-B bit sync design features an enhanced acquisition mode that greatly increases the speed of reacquisition when the incoming signal experience fades, dropouts, or other interruptions. By selecting the *Quick React Mode* command from the menu, the control loops that govern signal offset, AGC (automatic gain control), and the Costas Loop will go into a quasi "freeze" state whenever the PCM signal to the bit sync is interrupted. When the input signal resumes, the LS-40-B attempts to reacquire the signal with all of its internal loop states essentially the same as before the interruption. The Quick React Mode should not be used when the LS-40-B is trying to acquire a signal for the first time. For this reason, the Quick React Mode is always disabled when the Host application first starts running.



Output Controls

The extended functions feature allows the user to automatically disable the PCM and/or Tape outputs of the bit synchronizer during certain signal conditions. The user may select to disable the PCM output whenever the bit synchronizer is out of lock, and/or when the system E_s/N_0 level drops below 5 dB. The tape output of the bit synchronizer may be similarly controlled.

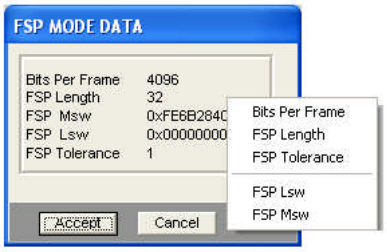
FSP Mode (Optional)

If the user has ordered this option, the LS-40-B bit sync will have the unique feature of being able to lock onto the frame sync pattern of an incoming signal. This feature can be unlocked by the factory. To achieve this, a frame synchronizer is employed with a correlator & state machine circuitry that recognize the unique bit patterns indicating the beginning of a minor frame of data. The frame synchronizer typically "searches" for patterns, "checks" for the recurrence of the pattern in the same position for several frame periods, and then "locks" on the pattern. To enable this feature, the user must select the *FSP Mode* command from the setup menu. A check mark next to the command will result indicating the status. Also note that when this function is enabled, the *Framesync Status*

Lock indicator will also appear in the Bitsync Status display window shown in **Error! Reference source not found.** on page **Error! Bookmark not defined.**.

FSP Mode Setup

There are four paremeters that must be specified for the FSP mode to operate correctly. These include: the length of the frame (*Bits Per Frame*), the length of the pattern (*FSP Length*), the FSP correlator tolerance (*FSP Tolerance*), and the frame sync pattern value (*FSP Msw/Lsw*).



Bits Per Frame

To define the major frame length in bits, the user must invoke the *Bits per Frame* command. The user must enter a length from 24 to 65,535 bits.

FSP Length.

To enter the required frame synchronization pattern, the user must first invoke the *FSP Length* command to specify the bit length of the frame sync pattern. The length of the pattern may be up to 64-bits.

FSP Tolerance

The user may specify the number of bits in the acquired sync pattern that may be different from the ideal pattern and still achieve & maintain synchronization by invoking the *FSP Tolerance* command. The user may specify that the received pattern must contain no bit errors, and would thus set the tolerance to Zero (0). In a noisy signal environment, such a setting would likely result in the LS-40-B NEVER acquiring or maintaining frame synchronization. For the noisy, real world environment, the user may set the bit error tolerance from 1 to 14 bits.

FSP Lsw/Msw

The frame synchronization pattern is a unique binary bit pattern used to indicate the beginning of a telemetry minor frame. To achieve this, a frame synchronizer is employed with a correlator & state machine circuitry that recognizes unique bit patterns indicating the beginning of minor frame data. The frame synchronizer typically "searches" for patterns, "checks" for the recurrence of the pattern in the same position for several frame periods, and then "locks" on the pattern. In this application, the frame synchronization pattern entered by the user in two, 32-bit words, designated as *FSP Msw* (most significant word) and *FSP Lsw* (least significant word).

4.1.1.1.1 BERT PRN Pattern

Selecting the proper PN sequence that will be appropriate for the particular system being tested is important. Some of the key properties of the selected PN sequence that are of

importance include: the length of the PN Sequence, the type of Linear Feedback Shift Register configuration used to implement the PN generator (this defines the binary run properties of the sequence), and the spectral line spacing of the sequence (which depends on the bit rate of the sequence). The user may select from one of seven (2) PN sequences by invoking the **PRN Pattern** command. Available pattern lengths include: 2^{11}-1, 2^{15}-1.

5 Programming

This chapter provides interface and setup information for the LS-40-B drive bay bit synchronizer.

5.1 Bus Interfaces

The LS-40-B is controlled via one of two standard RS/EIA serial interface methods: RS/EIA-232 or EIA/RS-485. The unit it shipped from the factory configured for control via an RS-232 interface.

5.1.1 RS-232 Interface Method

The RS-232 interface is the factory configured default interface method. This interface is capable of being run at rates between 9.6k BAUD and 115.2k BAUD with a default rate of 57.6k BAUD. In order for this interface method to be active, the configuration switches of SW1 have to be set as indicated: SW1-1 through SW1-4 switched to the OFF position. If SW1-5 is switched to the ON position, the module address switches are ignored and the unit is set to utilize the RS-232 interface at 57.6k BAUD.

5.1.2 RS-485 Interface Method (Future)

Details of this interface method will be provided in future firmware releases.

5.2 General Command and Status Messaging

The interface to the LS-40-B is implemented via command-response messaging. For every command sent from the host, the bit sync will respond to indicate that the command was received. Commands from the host are grouped in two categories: primary commands and secondary commands. Primary commands are used to control the basic setup of the bit sync. Secondary commands are used to set various "lower-priority" operational modes and to obtain secondary status. Secondary host commands occasionally require that the host send two commands: a first command followed by a status request message.

All host messages require a message header of six (6) bytes. If the host command requires additional data be transferred to the host, the data will immediately follow the command header. Figure 5-1 on page 27 contains a diagram of the message header for the LS-40-B.

The first byte of the message header contains a device identification flag of **0x40**. The second byte indicates the module address being commanded. For RS-232 communications, this should always be set to 0x00. The 3rd and 4th bytes contain the message identification. Message identification informs the LS-40-B the type and format of data that will follow the header, if any. Bytes 5 and 6 of the message header indicate the number of command related bytes that follow the message header.

In response to any host command, the LS-40-B will respond with a minimum of an echoed message header. If additional information is to be conveyed to the host, the data will immediately follow the echoed header. Figure 5-2 on page 28 indicates the general configuration of the host and terminal responses.

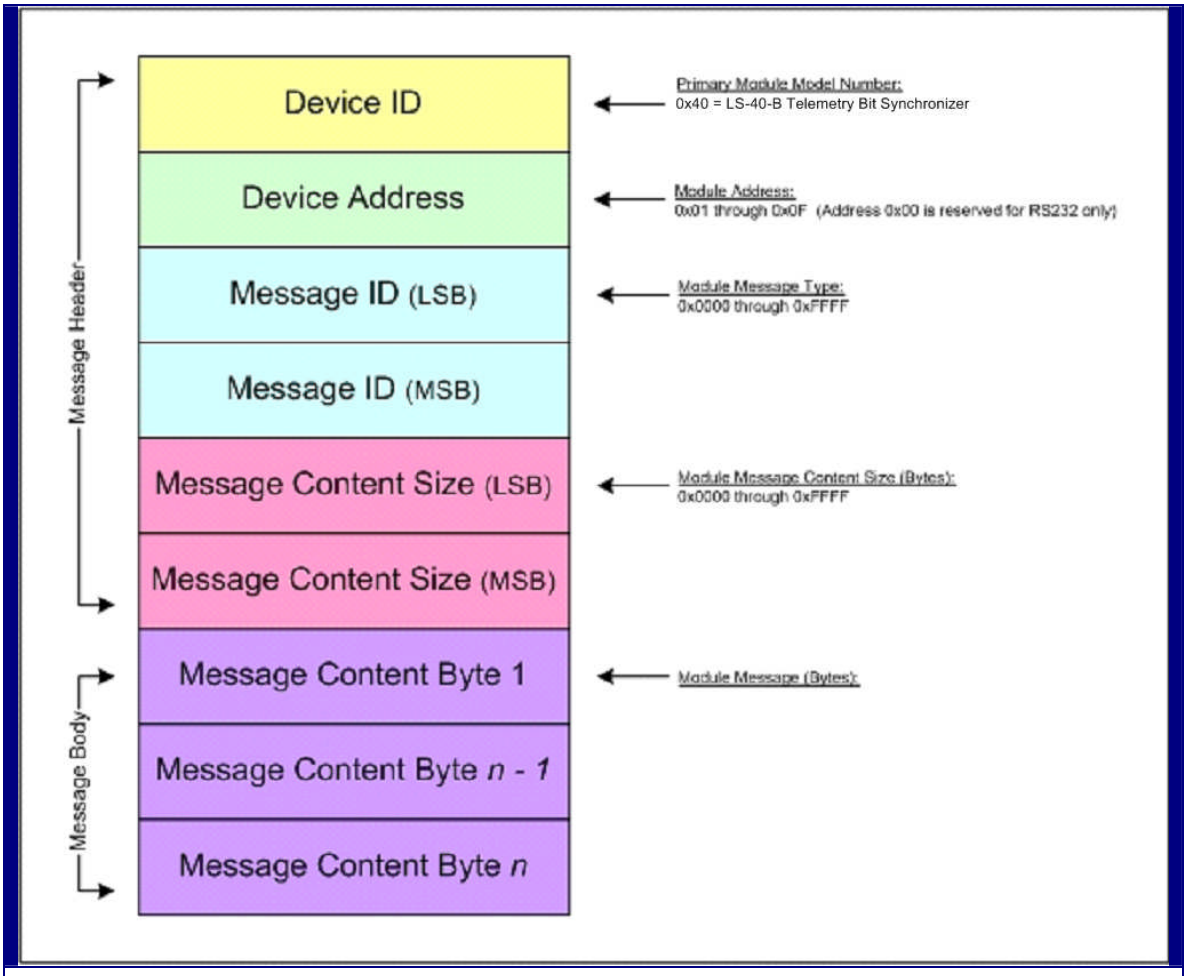


Figure 5-1 LS-40-B Message Format

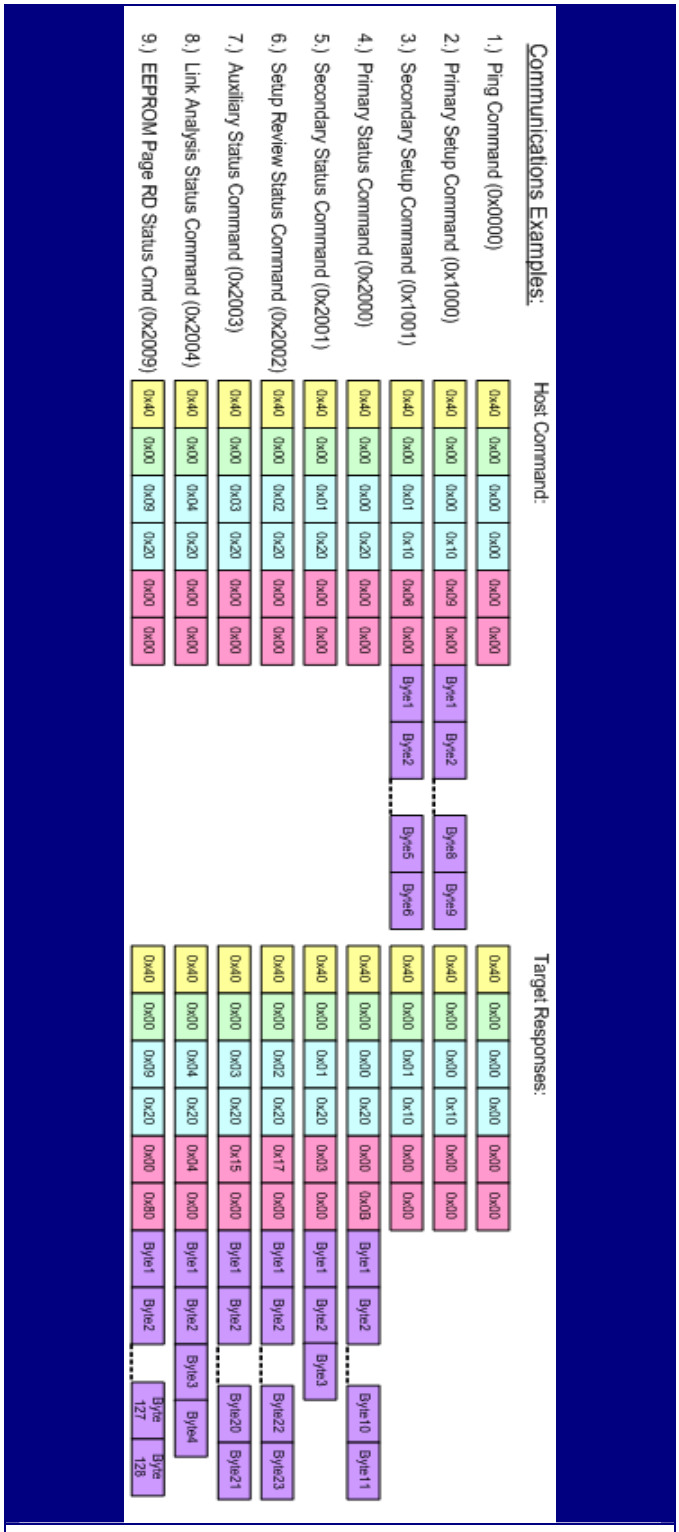


Figure 5-2 LS-40-B General Messaging Configurations

5.3 Command Messaging

There are three command message types: a "Ping" command, a "Primary Setup" command, and a "Secondary Setup" command.

5.3.1 The Ping Command

The "Ping" command is used to determine the health/presence of the communications channel between the host and the LS-40-B. In response to the "Ping" command, the LS-40-B will echo the received message header back to the host.

5.3.2 The Primary Setup Command

The "Primary Setup" command provides fundamental control information to the LS-40-B. The message header is followed by nine (9) data bytes as defined in Table 5-1 below.

Primary Command Message Content (Message ID = 0x1000)

Table 5-1 LS-40-B Primary Message Command Structure

Content Byte	D7	D6	D5	D4	D3	D2	D1	D0	Notes:
1	BRATE1								
2	BRATE2								
3	BRATE3								
4	BRATE4								
5	PCMIN								
6	PCMOUT								
7	LBW								
8	EACQ	RRC	FSENA	PRN	FORCE	LAENA	INPUT		
9	SNUM								

5.3.3 The Secondary Setup Command

The "Secondary Setup" command provides non-critical control information to the LS-40-B and requests the internal status from the LS-40-B. The message header is followed by six (6) data bytes as defined in Table 5-2 below.

Secondary Command Message Content (Message ID = 0x1001)

Table 5-2 LS-40-B Secondary Message Command Structure

Content Byte	D7	D6	D5	D4	D3	D2	D1	D0	Notes:
1	MODE								
2	CMD1								
3	CMD2								
4	CMD3								
5	CMD4								
6	CMD5								

5.3.4 Command Bit/Byte Definitions

Table 5-3 below contains the bit and bit pairing definitions for the primary and the secondary messages. Table 5-4 on page 31 contains the definition for the secondary message MODE byte.

Table 5-3 LS-40-B Command Bit Grouping Definitions

Command Mnemonic	Description/Definition	Logic State/Explanation
BRATE1	Programmed Bit Rate (MSW)	Bits 26-24 (Upper bits ignored….max bit rate >67Mbps)
BRATE2	Programmed Bit Rate	Bits 23-16
BRATE3	Programmed Bit Rate	Bits 15-8
BRATE4	Programmed Bit Rate (LSW)	Bits 7-0
PCMIN	PCM Input Decoder Select	0xA0 = NRZ-L 0xA1 = NRZ-M 0xA2 = NRZ-S 0xA3 = BIO-L 0xA4 = BIO-M 0xA5 = BIO-S 0xA6 = DM-M 0xA7 = DM-S 0xA8 = MDM-M 0xA9 = MDM-S 0xAA = INV NRZ-L 0xAB = INV BIO-L 0xAC = RZ 0xAD = INV RZ 0xAE = RNRZ11 0xAF = RNRZ15 0xD0 = RNRZ17 0xD1 = RNRZ23 0xD2 = INV NRZ-M 0xD3 = INV NRZ-S 0xD4 = INV BIO-M 0xD5 = INV BIO-S 0xD6 = INV DM-M 0xD7 = INV DM-S 0xD8 = INV MDM-M 0xD9 = INV MDM-S 0xDA = INV RNRZ11 0xDB = INV RNRZ15 0xDC = INV RNRZ17 0xDD = INV RNRZ23
PCMOUT	PCM Output Encoder Select	0xB0 = NRZ-L 0xB1 = NRZ-M 0xB2 = NRZ-S 0xB3 = BIO-L 0xB4 = BIO-M 0xB5 = BIO-S 0xB6 = DM-M 0xB7 = DM-S 0xB8 = MDM-M 0xB9 = MDM-S 0xBA = INV NRZ-L 0xBB = INV BIO-L 0xBC = RZ 0xBD = INV RZ 0xBE = RNRZ11 0xBF = RNRZ15 0xDE = RNRZ17 0xDF = RNRZ23
LBW	Loop Bandwidth	0x81 = 0.1% 0x82 = 0.2% 0x83 = 0.2% 0x84 = 0.2% 0x85 = 0.5% 0x86 = 0.5% 0x87 = 0.5% 0x88 = 1.0% 0x89 = 1.0% 0x8A = 1.0% 0x8B = 2.0% 0x8C = 2.0% 0x8D = 0.01% 0x8E = 0.02% 0x8F = 0.05%
INPUT	Input Source Select	00 = Primary Input 01 = Secondary Input 10 = Internal Loop-back 11 = (Unused)
LAENA	Link Analysis Enabled	0 = Disabled, 1= Enabled
FORCE	Link Analysis Forced Error	0 = Disabled, 1= Enabled
FSENA	Frame Sync Enabled	0 = Disabled, 1= Enabled
RRC	Raised Root Cosine Filter Enabled	0 = Disabled, 1= Enabled
PRN	Link Analysis PRN Source Select	0 = 2^{11}-1, 1 = 2^{15} - 1
EACQ	Enhanced Acquisition Enabled	0 = Disabled, 1= Enabled
SNUM	Setup Storage Number	(Value between 0 and 15)
MODE	Secondary Operations Mode Command	[See Table 5-4]
CMD1	Secondary Command Wd 1	[See Table 5-4]
CMD2	Secondary Command Wd 2	[See Table 5-4]
CMD3	Secondary Command Wd 3	[See Table 5-4]
CMD4	Secondary Command Wd 4	[See Table 5-4]
CMD5	Secondary Command Wd 5	[See Table 5-4]

Table 5-4 LS-40-B Secondary Command MODE Definitions

Definition	MODE	CMD1	CMD2	CMD3	CMD 4	CMD5
Null Mode	0x00	(Unused)	(Unused)	(Unused)	(Unused)	(Unused)
Frame Sync Pattern Mode (Optional)	0x01	*Pattern Sync Sub-Mode Select:* 0x00 = Pattern Bytes 1-4 0x01 = Pattern Bytes 5-8 0x02 = Pattern Setup	*Pattern-Sync Data:* Byte 1 (MSB of Pattern) Byte 5 Pattern Size (1-64)	*Pattern-Sync Data:* Byte 2 Byte 6 Sync Tolerance (0-14)	*Pattern-Sync Data:* Byte 3 Byte 7 Frame Bit Count (MSB)	*Pattern-Sync Data:* Byte 4 Byte 8 (LSB of Pattern) Frame Bit Count (LSB)
PCM Outputs Control Mode	0x02	*Output Setup:* 0xC4 = PCM Outs Disabled @ PLL Unlock 0xC5 = PCM Outs Disabled @ Es/No < 5dB 0xC6 = PCM Enc, Outs Disabled @ PLL Unlock 0xC7 = PCM Enc. Outs Disabled @ Es/No Unlock 0xC8 = Enable all PCM Outputs (default)	(Unused)	(Unused)	(Unused)	(Unused)
Stored Setup Review	0x05	*Stored setup number:* Value between 0-15	(Unused)	(Unused)	(Unused)	(Unused)
EEPROM Mode	0x07	*Mode:* 0x00 = Read PROM 0 0x10 = Read PROM 1 (Future expansion)	*PROM Page:* Value Between 0-15	*PROM Line:* Value Between 0-63 or 255 for page review	(Unused)	(Unused)

5.3.5 Secondary Mode Command Notes:

Following is some additional information about the secondary mode commands listed in Table 5-4 above.

The **Null Mode c**ommand is issued to spawn the completion of a particular command or as a means to return to a known state.

The **Stored Setup Review** command allows the examination of stored setups. The proper sequences of steps for this command are as follows:

1. Set the review mode command by writing a 0x05 to the MODE field.
2. Write the stored setup number for review to CMD1.
3. The host should then pull the 0x2002 command which indicates the configuration of the stored setup.

The conditional **PCM Outputs Control Mode** command allows the review of stored setups. The proper sequences of steps for this command are as follows:

1. Set the conditional PCM output mode command by writing a 0x02 to the MODE field.
2. Write the desired setting to CMD1.

The **Frame Sync Pattern Sync Mode** commands are a series of mode commands that allow the configuration of the Frame Sync parameters within the bit sync. This feature is an optional, factory installed option. The proper sequences of steps for this command are as follows:

1. First, set the first four bytes of the Sync Pattern (for this example -> FAF320 pattern, a 8192 bit frame size, with 1 bit of tolerance) by sending the following commands: MODE= 0x01, CMD1 = 0x00, CMD2 = 0xFA, CMD3= 0xF3, CMD4 = 0x20, CMD5 = 0x00.
2. Next, send the last four bytes of the Sync Pattern (for this example -> FAF320 pattern, a 8192 bit frame size, with 1 bit of tolerance) by sending the following commands: MODE = 0x01, CMD1 = 0x01, CMD2 = 0x00, CMD3 = 0x00, CMD4 = 0x00, CMD5 = 0x00.
3. Finally, send the frame sync setup information as shown below: MODE = 0x01, CMD1 = 0x02, CMD2 = 0x18, CMD3 = 0x01, CMD4 = 0x20, CMD5 = 0x00.

The *Read* **EEPROM Mode** command provides a means of reading from EEPROM pages. To invoke this command, perform the following setup:

1. Set the EEPROM mode by writing a 0x07 to the MODE field.
2. Select the EEPROM to be examined and the read function by writing a 0x00 or 0x10 to the CMD1 register. Only EEPROM 1 is currently installed.
3. Enter the EEPROM page number in CMD2.
4. Enter the EEPROM line number in CMD3. A 0xFF placed in this position provides page EEPROM responses via the 0x2009 status response message ONLY!
5. If the line number was 0 to 63, issue a 0x2001 status message to retrieve the contents of the EEPROM data. LSBs of the EEPROM content will be in RTN1 and MSBs of the PROM content will be in RTN2. If the line number was 0xFF, issue a 0x2009 EEPROM Page Status Command to retrieve the contents of the entire page.

5.4 Status Response

There are six status response messages including: a "Primary Status Message", a "Secondary Response Content", a "Stored Setup Status Message", an "Auxiliary Status Message", a "Link Analysis Status Message", and an "EEPROM Page Read Response Content." Each is documented in the following paragraphs.

5.4.1 Primary Status Response Message

The Primary Status Response message provides fundamental status information about the LS-40-B. The message header is followed by eleven (11) data bytes as defined in Table 5-5 below.

Primary Status Message (Message ID = 0x2000)

Table 5-5 LS-40-B Primary Status Response Message Structure

Content Byte	D7	D6	D5	D4	D3	D2	D1	D0	Notes:
1	-	-	SW6	SW5	MODID				
2	LALCK	LAENA	FSPDET	FSPENA	BIT	SQUAL	PLL	THRES	
3	D0								
4	S0								
5	P0								
6	W0								
7	D1								
8	S1								
9	P1								
10	W1								
11	SNUM								

5.4.2 Secondary Status Response Message

The Secondary Status Response message provides non-critical status information to the LS-40-B. The message header is followed by three (3) data bytes as defined in Table 5-6 below.

Secondary Status Response Content (Message ID = 0x2001)

Table 5-6 LS-40-B Secondary Status Response Message Structure

Content Byte	D7	D6	D5	D4	D3	D2	D1	D0	Notes:
1	MODE								
2	RTN1								
3	RTN2								

5.4.3 Stored Setup Response Message

A total of sixteen (16) bit sync setups can be stored in the LS-40-B's internal memory and then be recalled by simply providing an index value. (Future provisions will allow these setups to be activated via discrete interaction.) These configurations can be reviewed using the secondary mode commands. The stored setup status response message structure is shown in Table 5-7 below.

Stored Setup Status Message (Message ID = 0x2002)

Table 5-7 LS-40-B Stored Setup Response Message Structure

Content Byte	D7	D6	D5	D4	D3	D2	D1	D0	Notes:
1	BRATE1								
2	BRATE2								
3	BRATE3								
4	BRATE4								
5	PCMIN								
6	PCMOUT								
7	LBW								
8	EACQ	RCC	FSENA	PRN	FORCE	LAENA	INPUT		
9	FSYNC1								
10	FSYNC2								
11	FSYNC3								
12	FSYNC4								
13	FSYNC5								
14	FSYNC6								
15	FSYNC7								
16	FSYNC8								
17	FSYNC9								
18	FSYNC10								
19	FSYNC11								
20	FSYNC12								
21	PCMSTATE								
22	PRNVSET								
23	SNUM								

5.4.4 Auxiliary Status Response Message

The Auxiliary Status Response message provides fundamental signal health information about the signal input of the LS-40-B. The status includes for example: the bit count, an estimate of the input signal voltage, an estimate of the Es/N_0 for the signal, the frequency offset, frame sync status, as well as a variety of system voltage levels. The message header is followed by twenty one (21) data bytes as defined in Table 5-8 below.

Auxiliary Status Message (Message ID = 0x2003)

Table 5-8 LS-40-B Auxiliary Status Response Message Structure

Content Byte	D7	D6	D5	D4	D3	D2	D1	D0	Notes:
1	BCOUNT1								
2	BCOUNT2								
3	BCOUNT3								
4	BCOUNT4								
5	(*)SIGLVL1								
6	(*)SIGLVL2								
7	(*)SIGLVL3								
8	(*)SIGLVL4								
9	SIGLVLRNG								
10	(*)ESNO1								
11	(*)ESNO2								
12	(*)ESNO3								
13	(*)ESNO4								
14	(*)OFFSET1								
15	(*)OFFSET2								
16	(*)OFFSET3								
17	(*)OFFSET4								
18	FSPCNT1								
19	FSPCNT2								
20	-	-	-	-	-	-	TRK	PUB	
21	1P2VD	2P5VD	3P3VD	N5VA	P5VA	-	P12VD	P5VD	

5.4.5 Link Analysis Status Response Message

The Link Analysis Status Response message is associated with the BERT (bit error rate tester) function of the LS-40-B. Status includes: the link error count, correlator history, and error overflow count. The message header is followed by four (4) data bytes as defined in Table 5-9 below.

Link Analysis Status Message (Message ID = 0x2004)

Table 5-9 LS-40-B Link Analysis Status Response Message Structure

Content Byte	D7	D6	D5	D4	D3	D2	D1	D0	Notes:
1	LAERR1								
2	LAERR2								
3	LAERR3								
4	-	-	-	-	-	-	LAHIST	LAOFL	

5.4.6 EEPROM Page Read Response Content Message

The primary bit synchronizer configuration information, used to drive GUI software interface labels, is found in the first page (indexed from 0) of the LS-40-B's primary internal EEPROM. Information contained in this EEPROM includes the status of the PCM phase lock loop, input signal quality status, frame sync pattern detection status, input Es/N_0 estimates, along with various other configuration information. This

information can be accessed via an EEPROM read mode command. The resulting status message contents are shown in the Table 5-10.

EEPROM Page Read Response Content (Message ID = 0x2009)

Table 5-10 LS-40-B EEPROM Page Read Status Message Structure

Content Byte	D7	D6	D5	D4	D3	D2	D1	D0	Notes:
1	LOC0_LSB								
2	LOC0_MSB								
…	…								More bytes
127	LOC63_LSB								
128	LOC63_MSB								

5.4.7 Status Bit/Byte Definitions

Shown below, Table 5-11 contains the bit and bit pairing definitions for the LS-40-B status messages.

Table 5-11 LS-40-B Status Response Bit Grouping Definitions

Status Mnemonic	Description/Definition	Logic State/Explanation
SW5-6	Switch 5 and 6 Settings	Sw5 Indicates that the default RS232/57600 Mode switch is set; Sw6 Undefined
MODID	Module Serial ID	Value between 0 and 15; RS232 indicated by address 0
THRES	PCM Input Threshold Status	0 = Less than Threshold, 1= Greater than Threshold
PLL	PCM PLL Lock Status	0 = Unlocked, 1 = PLL Lock
SQUAL	Signal Quality Status	0 = Es/No < 5dB, 1 = Es/No > 5dB
BIT	Built-In-Test Status	0 = No BIT errors detected, 1 = BIT errors detected
FSPENA	Frame Sync Pattern Enabled Status	0 = Disabled, 1 = Enabled
FSPDET	Frame Sync Pattern Detected Status	0 = FSP Not detected, 1 = FSP detected
LAENA	Link-Analysis Enabled Status	0 = Disabled, 1 = Enabled
LALCK	Link-Analysis Lock Status	0 = Unlocked, 1 = Locked
D0	Definite "Zero" Confidence Status	(Value between 0 and 100)
S0	Strong "Zero" Confidence Status	(Value between 0 and 100)
P0	Potential "Zero" Confidence Status	(Value between 0 and 100)
W0	Weak "Zero" Confidence Status	(Value between 0 and 100)
D1	Definite "One" Confidence Status	(Value between 0 and 100)
S1	Strong "One" Confidence Status	(Value between 0 and 100)
P1	Potential "One" Confidence Status	(Value between 0 and 100)
W1	Weak "One" Confidence Status	(Value between 0 and 100)
SNUM	Setup storage Number	Value between 0 and 15
BCOUNT1	Bit Count Status (MSW)	Bits 26-24 (Upper bits ignored….max bit rate >67Mbps)
BCOUNT2	Bit Count Status	Bits 23-16
BCOUNT3	Bit Count Status	Bits 15-8
BCOUNT4	Bit Count Status (LSW)	Bits 7-0
(*)SIGLVL1	Input Signal Voltage Estimate	CSign (0x2D or 0x2B) [See example below]
(*)SIGLVL2	Input Signal Voltage Estimate	Component x10 [See example below]
(*)SIGLVL3	Input Signal Voltage Estimate	ESign (0x2D or 0x2B) [See example below]
(*)SIGLVL4	Input Signal Voltage Estimate	Exponent [See example below]
SIGLVLRNG	Input Signal Voltage Range Flag	0x30 < estimate shown, 0x31 = estimate shown, 0x32 > estimate shown
(*)ESNO1	Input Es/No Estimate	CSign (0x2D or 0x2B) [See example below]

Status Mnemonic	Description/Definition	Logic State/Explanation
(*)ESNO2	Input Es/No Estimate	Component x10 [See example below]
(*)ESNO3	Input Es/No Estimate	ESign (0x2D or 0x2B) [See example below]
(*)ESNO4	Input Es/No Estimate	Exponent [See example below]
(*)OFFSET1	Offset Frequency Status	CSign (0x2D or 0x2B) [See example below]
(*)OFFSET2	Offset Frequency Status	Component x10 [See example below]
(*)OFFSET3	Offset Frequency Status	ESign (0x2D or 0x2B) [See example below]
(*)OFFSET4	Offset Frequency Status	Exponent [See example below]
FSPCNT1	Frame Sync Count Status	Bits 15-8
FSPCNT2	Frame Sync Count Status	Bits 7-0
PUB	Power Up Bit Test Status	1 = Pass, 0 = Fail
TRK	PCM Input Track Status	1 = Pass, 0 = Fail
1P2VD	1.2V Digital Voltage Bus Status	1 = Pass, 0 = Out of Range
2P5VD	2.5V Digital Voltage Bus Status	1 = Pass, 0 = Out of Range
3P3VD	3.3V Digital Voltage Bus Status	1 = Pass, 0 = Out of Range
N5VA	-5V Analog Voltage Bus Status	1 = Pass, 0 = Out of Range
P5VA	5V Analog Voltage Bus Status	1 = Pass, 0 = Out of Range
P12VD	12V Digital Voltage Bus Status	1 = Pass, 0 = Out of Range
P5VD	5V Digital Voltage Bus Status	1 = Pass, 0 = Out of Range
LAERR1	Link-Analysis Error Count Status	Bits 19-16
LAERR2	Link-Analysis Error Count Status	Bits 15-8
LAERR3	Link-Analysis Error Count Status	Bits 7-0
LAOFL	Link Analysis Count Overflow Status	1 = Overflow, 0 = No Overflow Detected
LAHIST	Link-Analysis Correlator History Status	1 = Unlocked Since Last Update, 0 = Locked maintained since last update
BRATE1	Programmed Bit Rate (MSW)	Bits 26-24 (Upper bits ignored….max bit rate >67Mbps)
BRATE2	Programmed Bit Rate	Bits 23-16
BRATE3	Programmed Bit Rate	Bits 15-8
BRATE4	Programmed Bit Rate (LSW)	Bits 7-0
PCMIN	PCM Input Decoder Select	0xA0 = NRZ-L 0xA1 = NRZ-M 0xA2 = NRZ-S 0xA3 = BIO-L 0xA4 = BIO-M 0xA5 = BIO-S 0xA6 = DM-M 0xA7 = DM-S 0xA8 = MDM-M 0xA9 = MDM-S 0xAA = INV NRZ-L 0xAB = INV BIO-L 0xAC = RZ 0xAD = INV RZ 0xAE = RNRZ11 0xAF = RNRZ15 0xD0 = RNRZ17 0xD1 = RNRZ23 0xD2 = INV NRZ-M 0xD3 = INV NRZ-S 0xD4 = INV BIO-M 0xD5 = INV BIO-S 0xD6 = INV DM-M 0xD7 = INV DM-S 0xD8 = INV MDM-M 0xD9 = INV MDM-S 0xDA = INV RNRZ11 0xDB = INV RNRZ15 0xDC = INV RNRZ17 0xDD = INV RNRZ23
PCMOUT	PCM Output Encoder Select	0xB0 = NRZ-L 0xB1 = NRZ-M 0xB2 = NRZ-S 0xB3 = BIO-L 0xB4 = BIO-M 0xB5 = BIO-S 0xB6 = DM-M 0xB7 = DM-S 0xB8 = MDM-M 0xB9 = MDM-S 0xBA = INV NRZ-L 0xBB = INV BIO-L 0xBC = RZ 0xBD = INV RZ 0xBE = RNRZ11 0xBF = RNRZ15 0xDE = RNRZ17 0xDF = RNRZ23
LBW	Loop Bandwidth	0x81 = 0.1% 0x82 = 0.2% 0x83 = 0.2% 0x84 = 0.2% 0x85 = 0.5% 0x86 = 0.5% 0x87 = 0.5% 0x88 = 1.0% 0x89 = 1.0% 0x8A = 1.0% 0x8B = 2.0% 0x8C = 2.0% 0x8D = 0.01% 0x8E = 0.02% 0x8F = 0.05%
INPUT	Input Source Select	00 = Primary Input 01 = Secondary Input 10 = Internal Loop-back 11 = (Unused)
LAENA	Link Analysis Enabled	0 = Disabled, 1= Enabled
FORCE	Link Analysis Forced Error	0 = Disabled, 1= Enabled
FSENA	Frame Sync Enabled	0 = Disabled, 1= Enabled
RRC	Raised Root Cosine Filter Enabled	0 = Disabled, 1= Enabled
PRN	Link Analysis PRN Source Select	0 = 2^{11}-1, 1 = 2^{15} - 1
EACQ	Enhanced Acquisition Enabled	0 = Disabled, 1= Enabled

Status Mnemonic	Description/Definition	Logic State/Explanation
FSYNC1	Frame Sync Pattern Wd1 Setup	Frame Sync Pattern Wd1 Setup
FSYNC2	Frame Sync Pattern Wd2 Setup	Frame Sync Pattern Wd2 Setup
FSYNC3	Frame Sync Pattern Wd3 Setup	Frame Sync Pattern Wd3 Setup
FSYNC4	Frame Sync Pattern Wd4 Setup	Frame Sync Pattern Wd4 Setup
FSYNC5	Frame Sync Pattern Wd5 Setup	Frame Sync Pattern Wd5 Setup
FSYNC6	Frame Sync Pattern Wd6 Setup	Frame Sync Pattern Wd6 Setup
FSYNC7	Frame Sync Pattern Wd7 Setup	Frame Sync Pattern Wd7 Setup
FSYNC8	Frame Sync Pattern Wd8 Setup	Frame Sync Pattern Wd8 Setup
FSYNC9	Frame Sync Pattern Length Status	Value Between 1-64 Bits
FSYNC10	Frame Sync Pattern Tolerance Status	Value Between 0-14 Bits
FSYNC11	Frame Pattern Bit Count (MSW)	Bits 15-8
FSYNC12	Frame Pattern Bit Count (LSW)	Bits 7-0
PCMSTATE	PCM Output State Status	0xC4 = PCM Outputs Disabled @ PLL Unlock 0xC5 = PCM Outputs Disabled @ Es/No<5dB 0xC6 = PCM Enc. Out Disabled@ PLL Unlock 0xC7 = PCM Enc. Out Disabled@ Es/No<5dB 0xC8 = Enable all PCM Outputs
PRNVSET	PRN Programmed Output Voltage	Value between 0 and 100
MODE	Secondary Operations Mode Command	[See Operational Mode Table]
RTN1	Secondary Status Wd 1	[See Operational Mode Table]
RTN2	Secondary Status Wd 2	[See Operational Mode Table]
LOC0_LSB	EEPROM Contents – LSB	EEPROM Page Content Data Byte
LOC0_MSB	EEPROM Contents – MSB	EEPROM Page Content Data Byte
LOC63_LSB	EEPROM Contents – LSB	EEPROM Page Content Data Byte
LOC63_MSB	EEPROM Contents – MSB	EEPROM Page Content Data Byte

(*) Base 10 Floating point number representation:

Example 1.2×10^{-2}

CSign = negative = ASCII "-" = 0x2D
Component *10 = 1.2*10 = 12
ESign = negative = ASCII"-" = 0x2D
Exponent = 2

5.4.8 Configuration EEPROM MAP (Page zero)

Table 5-12 LS-40-B EEPROM Map (page-0)			
EEPROM Address			
Offset (Hex)	**Offset (Dec)**	**Register Contents**	**LS40B Defaults**
0x00	**0**	PRN Output Lower Vp-p Value (x 0.01V) [0 commanded to DAC]	0
0x01	**1**	PRN Output Upper Vp-p Value (x 0.01V) [100 commanded to DAC]	400
0x02	**2**	PRN Output Impedance (ohms)	50
0x03	**3**	Internal Bit Sync FPGA Firmware Version:	0
0x04	**4**	Internal Bit Sync Parallel Port Device ID (Identical to Line 12):	0x42
0x05	**5**	Internal Bit Sync DSP Firmware Version (MSB):	0
0x06	**6**	Internal Bit Sync DSP Firmware Version (Middle byte):	0
0x07	**7**	Internal Bit Sync DSP Firmware Version (LSB):	0
0x08	**8**	*(Unused)*	0
0x09	**9**	*(Unused)*	0
0x0A	**10**	Internal Bit Sync Pg1 Prom Line 0 – Serial Number Prefix (ASCII Letter):	'H'
0x0B	**11**	Internal Bit Sync Pg1 Prom Line 1 – Serial Number Suffix (number):	0
0x0C	**12**	Internal Bit Sync Pg1 Prom Line 2 – Parallel Port Device ID:	0x42
0x0D	**13**	Internal Bit Sync Pg1 Prom Line 3 – Internal EPROM Auto program	0
0x0E	**14**	Internal Bit Sync Pg1 Prom Line 4 – Auxiliary Input Single-Ended (0 = differential)	1
0x0F	**15**	Internal Bit Sync Pg1 Prom Line 5 – FSP Mode Enabled	1
0x10	**16**	Internal Bit Sync Pg1 Prom Line 6 – Indicator Traces Present	0
0x11	**17**	Internal Bit Sync Pg1 Prom Line 7 – Link Analysis Enabled	1
0x12	**18**	Internal Bit Sync Pg1 Prom Line 8 – Bit Slicer Status Enabled	1
0x13	**19**	Internal Bit Sync Pg1 Prom Line 9 – Bit Slicer 8 Byte Status Format (0 = 4 bytes)	1
0x14	**20**	Internal Bit Sync Pg1 Prom Line 10 – 25Mbps Mods installed (1 = installed)	0
0x15	**21**	Internal Bit Sync Pg1 Prom Line 11 – Drive Bay Form Factor (0 = traditional)	1
0x16	**22**	*(Unused)*	0
0x17... 0x2A	**23….42**	*(Unused)*	0
0x2B	**43**	*(Unused)*	0
0x2C	**44**	Max. Preset Number (Indexed from 0)	15
0x2D	**45**	Active Setup at Boot	0
0x2E	**46**	*(Unused)*	0
0x2F	**47**	*(Unused)*	0
0x30	**48**	Controller FPGA Firmware Version ID:	(0-255)
0x31	**49**	Controller DSP Firmware Version ID (Year):	0x2007
0x32	**50**	Controller DSP Firmware Version ID (Mo/Day):	0x0909
0x33	**51**	Assembly Serial Number MSW: (Typically an ASCII Character)	(MSW)
0x34	**52**	Assembly Serial Number LSW: (Typically a number)	(LSW)
0x35	**53**	Brick Primary Function Designator	40
0x36	**54**	Brick Options Configuration Character #1 (ASCII Character)	ASCII "Null"
0x37	**55**	Brick Options Configuration Character #2 (ASCII Character)	ASCII "Null"
0x38	**56**	*(Unused)*	0
0x39	**57**	BAUD Rate (x100 bps): [Valid between 9600 and 2.5Mbps]	576
0x3A	**58**	Serial Communications Format: (485 = RS485, 232 = RS232)	232
0x3B	**59**	Serial Slew Rate (1= Fast, 0 = Slow)	1
0x3C	**60**	*(Unused)*	0
0x3D	**61**	*(Unused)*	0
0x3E	**62**	*(Unused)*	0
0x3F	**63**	*(Unused)*	0