LS-25-D and LS-25 - Version 2

Hardware User's Manual

Multi-band RF Downconverter and AM/FM Receiver

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TABLE OF CONTENTS

List of Tables

List of Figures

1 Introduction

1.1 General

This document is the Hardware User's Manual for the Version 2 Lumistar LS-25-D Multi-band RF Downconverter and the LS-25 Multi-band FM Receiver. These products represent Lumistar's 2nd generation of RF receiver designs that have replaced the original LS-25 receiver series. Figure 1-1 on page 8 contains detailed model number construction. This document applies to all model combinations indicated by this figure. The original product line is described in User Manual U250401. Consult the factory for a copy of this document.

The intent of this document is to provide physical, functional, and operational information for the end user including hardware configuration, interconnection and software interfaces for the device.

Both receivers implement a switching dual/single-superhetrodyne receiver design. The designs provide for the Downconversion for up to three RF bands, providing two 70MHz second intermediate frequency (IF) outputs as well as AM demodulation of the input signal. The product may be configured with up to 12 IF bandwidth filters. In addition to the functions of the LS-25-D, the LS-25 provides an additional FM demodulation stage and up to12 selectable video filters applied to the demodulated PCM signal.

Table 1-1 on page 9 provides specifications for electrical, mechanical, and operational characteristics of the LS-25-D and LS-25 receiver product line. A block diagram of the receiver is shown in Figure 1-2 on page 10.

1.2 Manual Format and Conventions

This manual contains the following sections:

- Chapter 1 provides a brief product overview and technical specifications
- Chapter 2 provides receiver theory of operation
- Chapter 3 provides installation and configuration instructions
- Chapter 4 provides info on the LS-25/25-D LDPS software application
- Chapter 5 provides programming information

Throughout this document, several document flags will be utilized to emphasis warnings or other important data. These flags come in three different formats: Warnings, Cautions, and Information. Examples of these flags appear below.

Warning:

(Details of critical information which prevents loss of functionality)

Caution:

Details of operational or functional cautionary advisories

Information:

(Details of emphasised operational information)

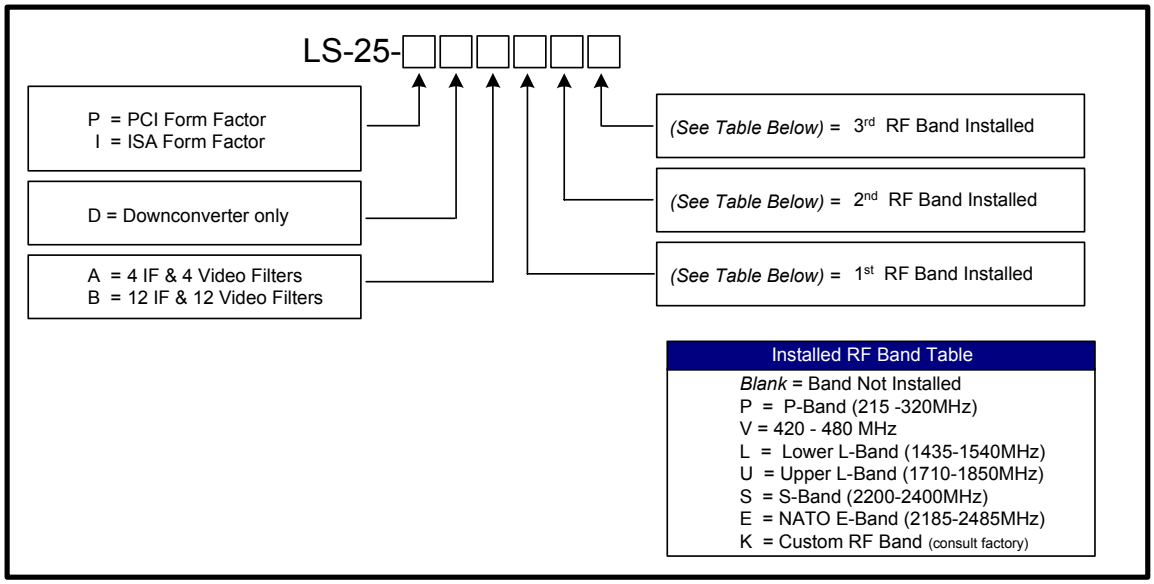


Figure 1-1 LS-25-D/LS-25 Model Number Construction Details[1]

[1] Note: in the ISA configuration, only 4 IF filters and one band are available.

Category:	Specifications:	Details:
Mechanical		
	Envelope Dimensions	12.35"(L) x 4.01"(W) x 0.62" (H) - PCI 13.37"(L) x 3.90"(W) x 0.62" (H) - ISA
	Form Factor	Full-length PCI or Full-length ISA
	Weight	~ 24oz.
Electrical		
	Individual power requirements	+5VDC @ 325mA
		+12VDC @ 530mA
		-12VDC @ 215mA
	Total Power	< 10.6 Watts
Performance		
RF Tuner	RF Input Bands	2185.5 - 2485.5 MHz (NATO E-Band)
		2200.5 - 2399.5 MHz (S-Band)
		1710.5 - 1849.5 MHz (Upper L-Band)
		1435.5 - 1539.5 MHz (Lower L-Band)
		215.5 - 319.5 MHz (P-Band)
		Custom (Consult Factory)
	Tuner Resolution	50kHz
	Frequency Accuracy	0.002% (Max.) 0.001% (Typical)
	RF Input AGC Range	-20dBm to –90dBm
	Input Level without Damage	+18dBm
	Receiver Input P_{1dB}	-10dBm (typical)
	Receiver Noise Figure	5dB (typical) / 8dB (maximum)
	70MHz Phase Noise @ 100kHz	Less than -102dBc, -110dBc (typical)
	Receiver OIP_3	> +15dBm (typical)
	70MHz Output Level	-20dBm (+/- 1dBm)
	2nd IF 3dB Bandwidths Available	500kHz, 1MHz, 1.5MHz, 2.5MHz, 3.5MHz, 4MHz, 6MHz, 8MHz, 10MHz, 12MHz, 16MHz, 20MHz *(Others Available - 2MHz, 3MHz, 4.5MHz, 5MHz, 7MHz, 9MHz, 14MHz, 18MHz, 22MHz, 24MHz, 26MHz, 28MHz, 30MHz, 36MHz Consult factory)*
Demodulation	Types	LS-25-D AM Only; LS-25 AM/FM
	AM Frequency Response	50kHz (AM Low-pass Bypass Mode)
	AM 6dB Low-pass Filters	50 Hz, 500 Hz, 5000 Hz, Bypass
	FM Deviation Range	75kHz -13MHz peak
	Video Filter 1dB Bandwidths	250kHz, 500kHz, 750kHz, 1.25MHz, 1.75MHz, 2MHz, 3MHz, 4MHz, 5MHz, 6MHz, 8MHz, 10MHz *(Custom - Consult Factory)*
Connectors		
	20MHz Reference Input/Output	SMB Male (J1)
	RF Signal Input	SMA Female (J2)
	Accessory I/O Connector	Molex 14-pin Connector (J3)
	Hybrid D-Style Connector	Mixed Discrete and Coax Connections (J5)
Environmental		
	Temperature, Operational	0° to 70° C (Commercial)
	Temperature, Storage	-20° to 70° C
	Humidity, non-condensing	<40° C 0-90%, >40° C 0-75%

Table 1-1 Specifications for the LS-25-D/LS-25 Series Multi-band Receivers

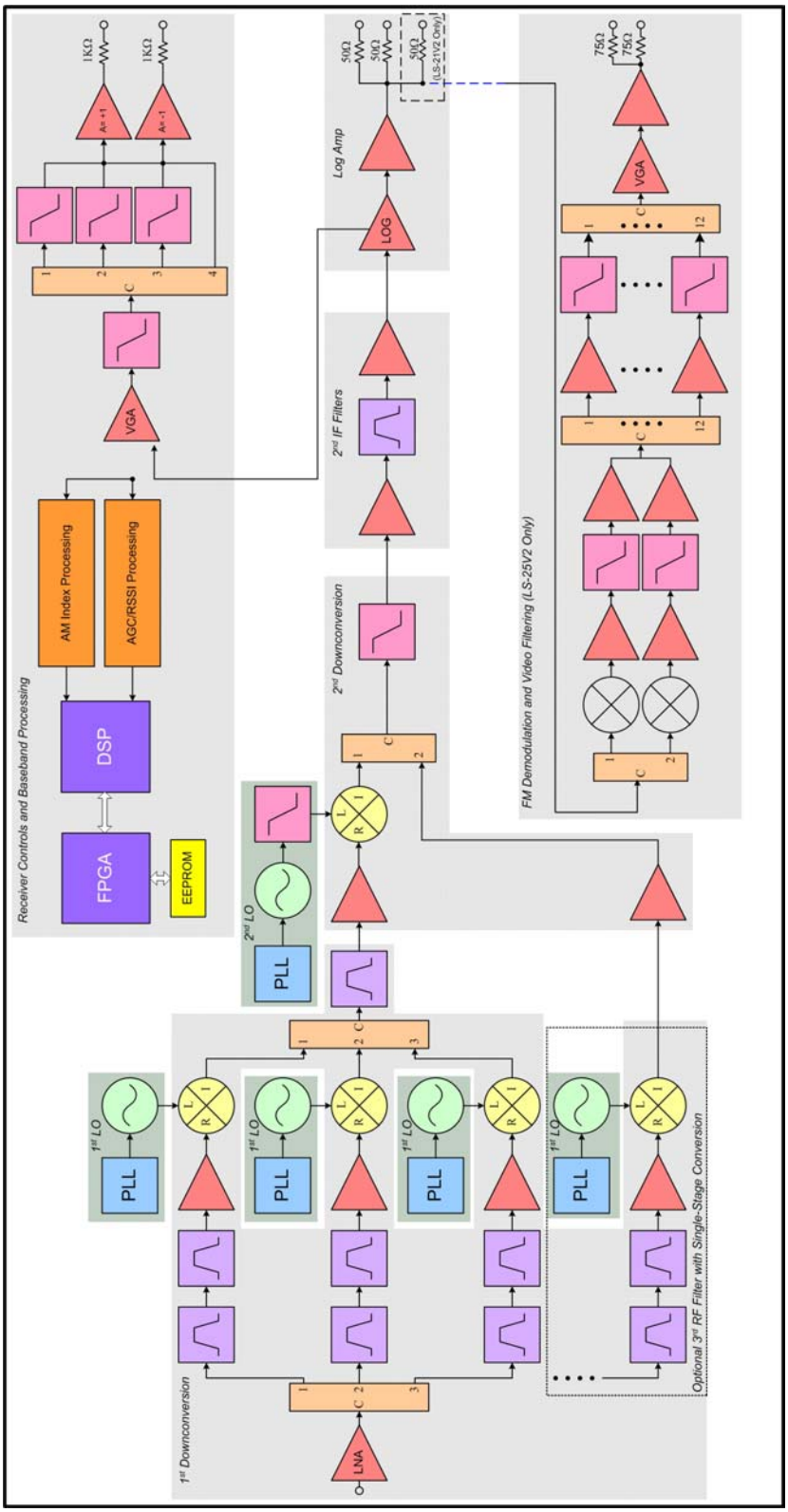


Figure 1-2 Block Diagram of the LS-25-D/LS-25 Series Multi-band Receivers

2 Theory of Operation

In order to more clearly understand the operation of the receivers, this section will detail the various sections of the receiver. The designs include nine primary stages:

- 1st Downconversion / 1st IF Band-pass Filter
- 1st Local Oscillator
- 2nd Downconversion
- 2nd Local Oscillator
- 2nd IF Filter
- Logarithmic Amplifier/AM Demodulation
- FM Demodulation
- Post Detect (Video) Filter

Each of these sections are physically shielded and isolated from one another to facilitate the greatest EMI/RFI ingress and egress protection allowing the receiver exceptional performance.

For the following sections, refer to the block diagram of Figure 1-2 on page 10.

2.1 1st Downconversion

The RF input is applied to the 1st Downconversion stage. This stage contains a low-noise amplifier (LNA) to provide a large amount of gain enhancing the receiver's overall sensitivity. Selectable RF band-pass filters follow the LNA. The RF signal is then mixed with the first local oscillator (LO) which coverts it to a lower frequency, referred to as the 1st IF frequency. Finally, the signal is applied to a 45MHz band-pass filter to limit the overall noise bandwidth applied to the remaining receiver sections.

2.2 1st Local Oscillator

In a superhetrodyne design, local oscillators (LOs) are utilized to convert high frequencies to lower, "intermediate" frequencies. The first LO is injected into the mixer of the first Downconversion stage to accomplish this task. Mixers can either utilize a sum or difference frequency component to produce IF frequencies. For example, if an RF frequency of 2,200 MHz was to be converted to an intermediate frequency of 250MHz, a difference component of 1,950MHz could injected to the mixer or a sum frequency component of 2,450MHz could be applied. The difference component LO application is referred to a "low-side" conversion. The sum component application is referred to as "high-side" conversion. Both methods are equally valid and each has its own benefits. The LS-25-D and LS-25 designs utilize low-side conversion to prevent spectral inversions.

2.3 2nd Downconversion

The receiver designs contain a switchable 2nd Downconversion stage. Similar to the 1st Downconversion stage, it contains a mixer to convert the 1st IF frequency to a second IF frequency of 70MHz. If the RF frequency band is relatively low, as is the case for P-Band inputs, the on-board processor can bypass the 2nd Downconversion stage switching to a single superhetrodyne process. In either case, a low-pass filter is applied to the signal path at the output of this stage to reduce harmonics and low frequency noise from being applied to subsequent stages.

2.4 2nd Local Oscillator

The second LO is injected into the mixer of the 2nd Downconversion stage to provide the second IF frequency of 70MHz. Like the first conversion stage, the second LO utilizes low-side injection for this conversion. A low-pass filter is applied to the LO output to minimize spurious and harmonic signals from being converted in the 2nd Downconversion stage. The 2nd LO is automatically disabled for RF bands that employ a single super heterodyne process.

2.5 2nd IF Filter

From the output of the 2nd conversion stage, the resulting intermediate frequency is then applied to a group of bandpass filters. The 2nd IF stage contains 4 or 12 IF (SAW) filters centered at 70MHz and varying in bandwidth from 500kHz to 36MHz.

2.6 Logarithmic Amplifier/AM Demodulation

Outputs from the 2nd IF Filter Stage are routed to the final gain stage in the receiver. A Logarithmic Amplifier acts as the main system gain element providing from 70 to 100dB of signal gain. In addition this stage provides received signal strength detection and AM demodulation.

2.7 FM Demodulation (LS-25 Receiver Versions ONLY)

The LS-25 versions of the receiver contain a dual FM discriminator design. Two discriminators are utilized to optimize the resulting baseband production based on signal deviation levels. A narrow deviation signal discriminator is utilized for signals that have peak deviations of less than 1MHz. A separate discrimination stage is utilized for signals with peak deviations greater than 1MHz. Following each discrimination stage, a low-pass filter is utilized to minimize baseband noise and IF frequency bleed-through. Selection of the discriminator stages is performed automatically based on the user programming selections.

2.8 Post Detection (Video) Filter (LS-25 Receiver Versions ONLY)

The LS-25 versions of the receiver contains twelve video filters to further filter the baseband PCM signal, reducing the noise bandwidth of the output signal. Default video filters are roughly half the bandwidth of the IF filters but can be varied for specific applications. Consult the factory for custom video filter bandwidths.

3 Installation and Configuration

Chapter 3 provides installation and configuration information. This chapter will locate serial numbers and product configuration information, familiarize the user with the layout of the board, and provide information on the proper installation and interconnection of the hardware.

3.1 Product Outline Diagrams

Figure 3-1 on page 14 contains an outline diagram of the top and bottom sides of the PCI versions of the product. Figure 3-2 on page 15 contains an outline diagram of the top and bottom sides of the ISA version of the product. Connector locations and switch positions are indicated. The model number, serial number, revision information and product options are denoted on the upper edge of the RF enclosure as indicated in the two figures.

3.2 Hardware Configuration

The receiver design contains configuration switches to control various functions, and in the case of the ISA format, to provide addressing of the board. Figure 3-3 on page 16 contains a diagram of the configuration switches along with the default factory positions for these switches.

Warning:
Switches indicated as FACTORY USE ONLY should not be altered from the indicated positions to ensure proper receiver operation.

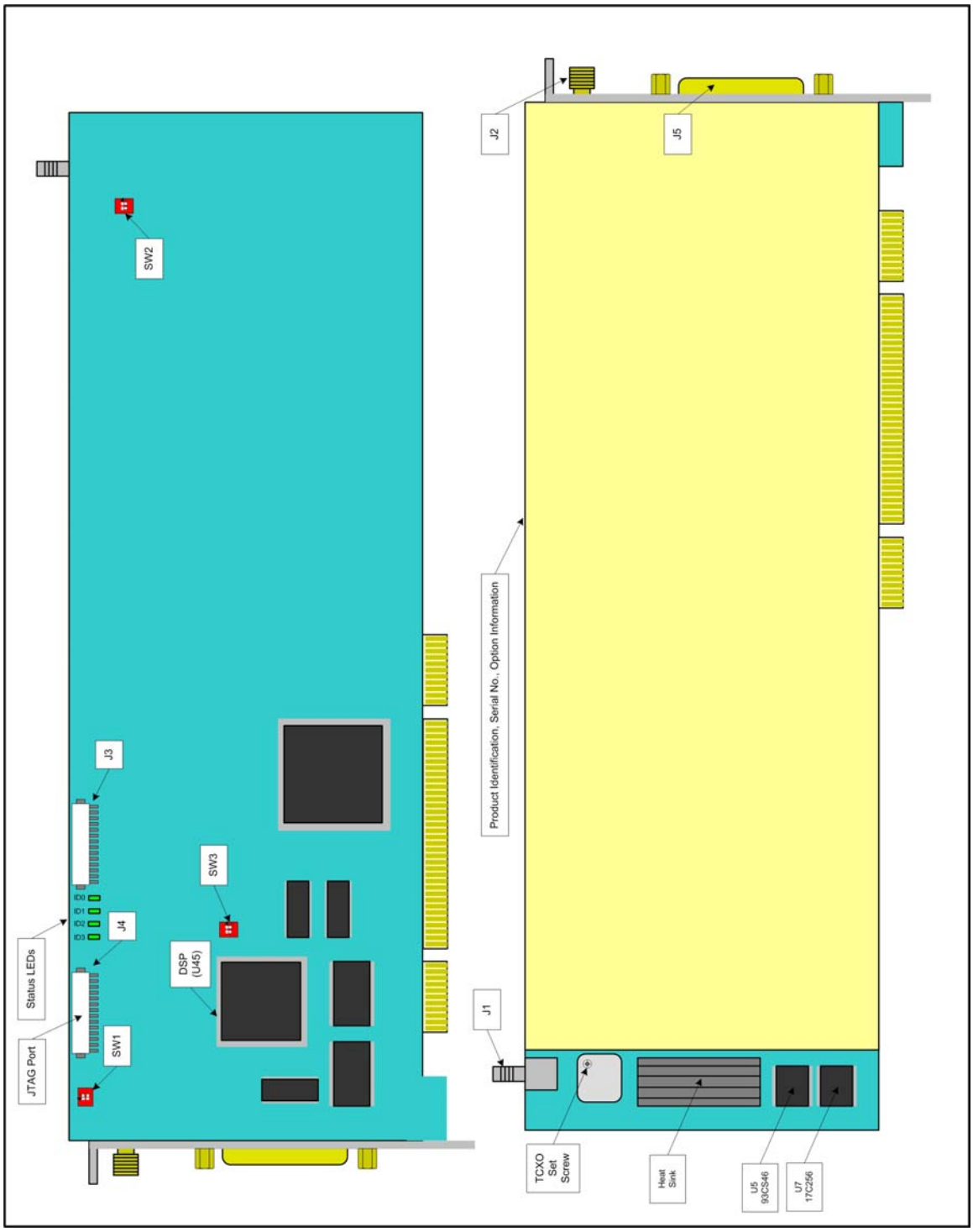


Figure 3-1 LS-25/LS-25-D PCI Outline Drawing

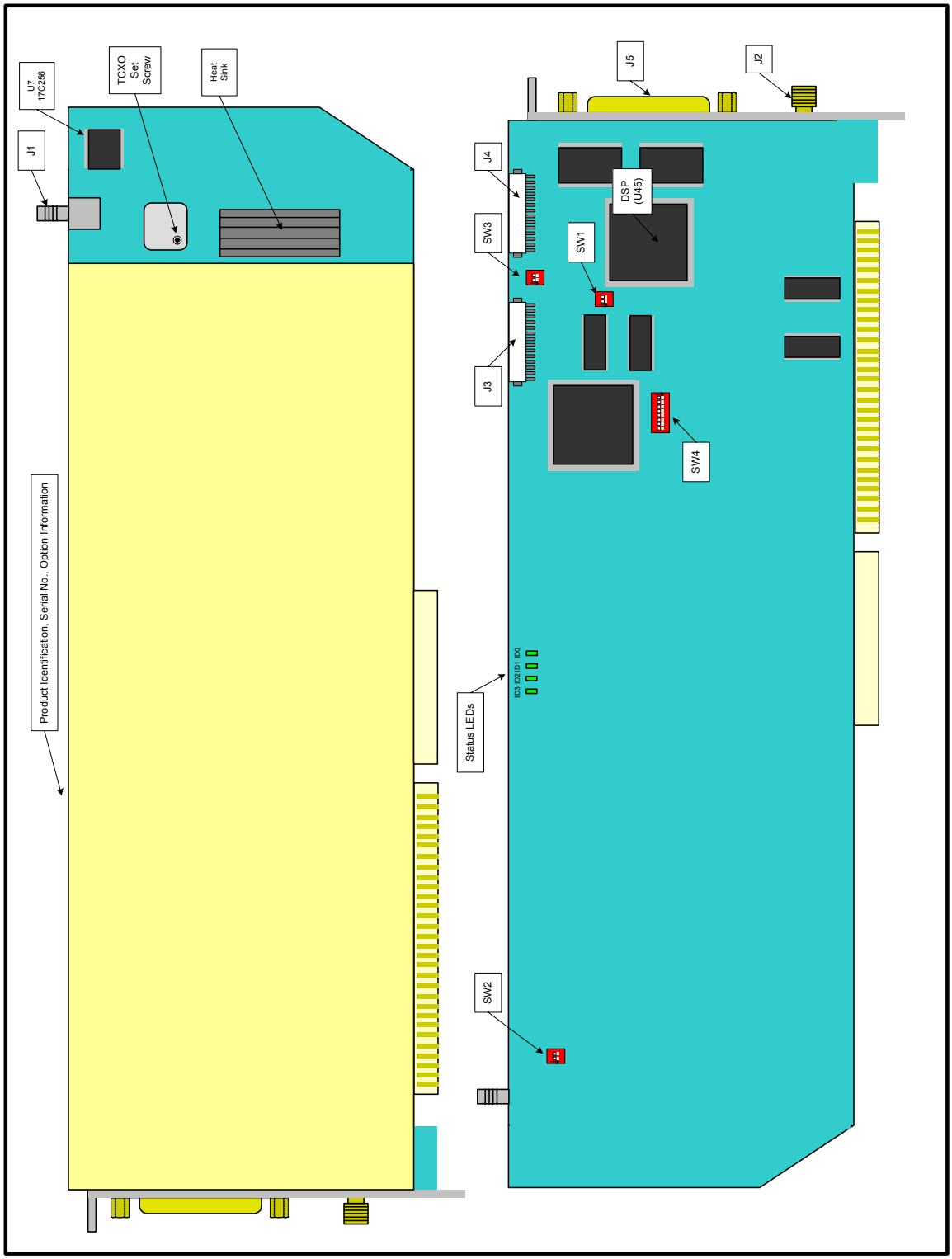


Figure 3-2 LS-25/LS-25-D ISA Outline Drawing

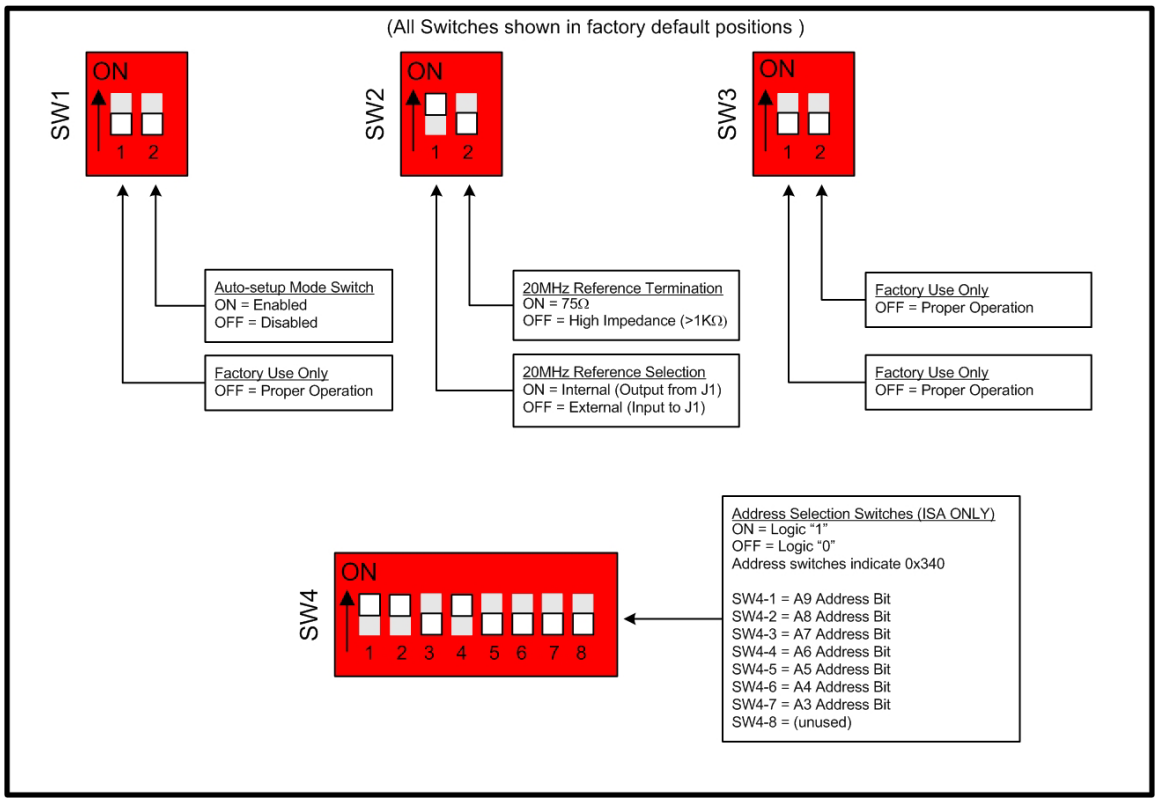


Figure 3-3 Receiver Configuration Switches

3.3 Physical Installation

To install the receiver in the target computer system, the following procedure should be followed:

1. Perform a normal system shutdown of the PC system and remove the primary power plug.

Warning:
Installation of the receiver in a powered platform will cause immediate damage to the interface hardware. Ensure that power is removed from the system prior to hardware installation.

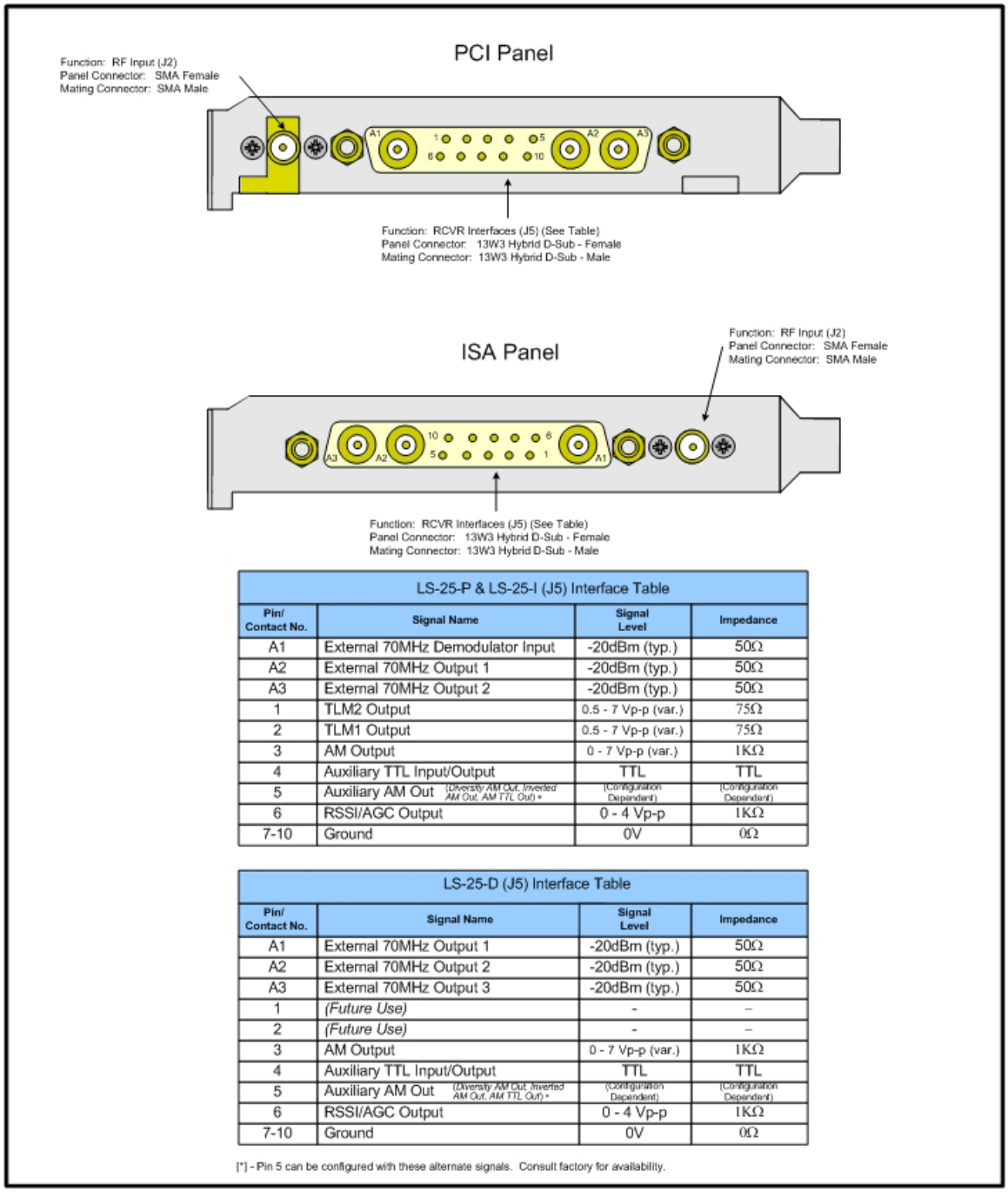
2. Install the receiver in an unobstructed full-length PC slot ensuring that the receiver is properly seated in the interface bus socket. PCs vary in their mechanical configurations so it may be necessary to remove additional PC hardware to properly install the receiver. For PCI installations, it may be necessary to remove the blue ISA extension bracket at the rear of the PCI card, depending on the mechanical configuration of your particular platform.

3. Install a screw in the mounting panel to secure the unit. If the unit is installed in a portable or rack mount PC, it may also be necessary to secure the rear of the board to the chassis of the PC via standard self-locking cable ties. Some platforms also have a vertical hold down which can be adjusted to provide additional mechanical stability.

3.4 Interconnection

The receiver platforms provide four interface connectors. For the typical application, only the J2 and J5 connectors are required. For use in a diversity combiner circuit, or for use with a high-stability external reference source, J1 is provided. The J3 connector provides special auxiliary interfaces and is typically unused. Receivers are shipped without the J3 connector installed unless requested by the customer. Figure 3-4 on page 18 provides interface pin-outs and mating connector information for the J2 and J5 connectors. Figure 3-5 on page 19 provides interface pin-outs and mating connector information for the J3 connector.

The LS-25 and LS-25-D products are shipped with a mating pigtail cable to interface with the J5 connector. Figure 3-6 on page 20 illustrates these cable configurations.



LS-25-P & LS-25-I (J5) Interface Table			
Pin/ Contact No.	**Signal Name**	**Signal Level**	**Impedance**
A1	External 70MHz Demodulator Input	-20dBm (typ.)	50Ω
A2	External 70MHz Output 1	-20dBm (typ.)	50Ω
A3	External 70MHz Output 2	-20dBm (typ.)	50Ω
1	TLM2 Output	0.5 - 7 Vp-p (var.)	75Ω
2	TLM1 Output	0.5 - 7 Vp-p (var.)	75Ω
3	AM Output	0 - 7 Vp-p (var.)	1KΩ
4	Auxiliary TTL Input/Output	TTL	TTL
5	Auxiliary AM Out *(Diversity AM Out, Inverted AM Out, AM TTL Out)* *	(Configuration Dependent)	(Configuration Dependent)
6	RSSI/AGC Output	0 - 4 Vp-p	1KΩ
7-10	Ground	0V	0Ω

LS-25-D (J5) Interface Table			
Pin/ Contact No.	**Signal Name**	**Signal Level**	**Impedance**
A1	External 70MHz Output 1	-20dBm (typ.)	50Ω
A2	External 70MHz Output 2	-20dBm (typ.)	50Ω
A3	External 70MHz Output 3	-20dBm (typ.)	50Ω
1	*(Future Use)*	-	–
2	*(Future Use)*	-	–
3	AM Output	0 - 7 Vp-p (var.)	1KΩ
4	Auxiliary TTL Input/Output	TTL	TTL
5	Auxiliary AM Out *(Diversity AM Out, Inverted AM Out, AM TTL Out)* *	(Configuration Dependent)	(Configuration Dependent)
6	RSSI/AGC Output	0 - 4 Vp-p	1KΩ
7-10	Ground	0V	0Ω

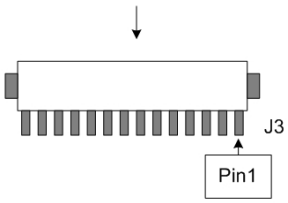
[*] - Pin 5 can be configured with these alternate signals. Consult factory for availability.

Figure 3-4 J2/J5 Pin-out and Interface Connections

Caution:

When utilizing the supplied pigtail, ensure that the three hybrid coax contacts are properly aligned with the J5 mating connector to prevent contact damage.

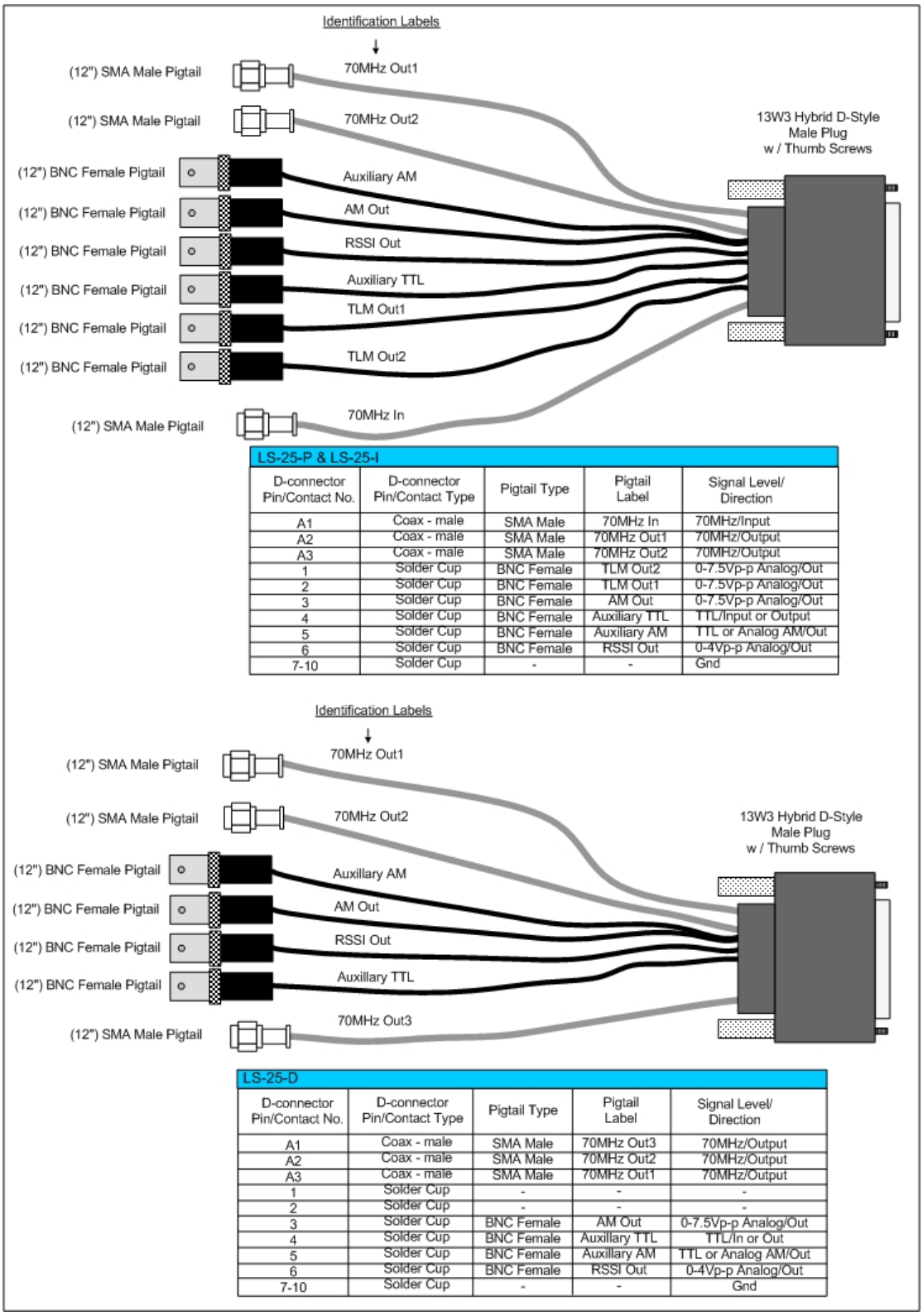
Function: Accessory Interfaces (See Table Below)
Panel Connector: 53780-1400 (Molex)
Mating Connector: 51146-1400 (Molex)



J3 Interface Table

Pin/ Contact No.	Signal Name	Signal Level	Impedance
1	-5VDC Power Source	-5VDC	-
2	Accessory Output 1	TTL	TTL
3	Accessory Output 2	TTL	TTL
4	Ground	0V	0Ω
5	RS-232 Serial Data Transmit	RS-232	–
6	FM Deviation Output (LS-25V2 Only)	0 - 3.3VDC	1KΩ
7	Ground	0V	0Ω
8	RSSI Output	0 - 4 Vp-p	1KΩ
9	Ground	0V	0Ω
10	AM TTL Output	TTL	TTL
11	RS-232 Serial Data Receive	RS-232	-
12	Reference Output/Input	20MHz/~1 Vp-p	75Ω
13	Ground	0V	0Ω
14	+5VDC Power Source	+5VDC	–

Figure 3-5 J3 Pin-out and Interface Connections



LS-25-P & LS-25-I

D-connector Pin/Contact No.	D-connector Pin/Contact Type	Pigtail Type	Pigtail Label	Signal Level/ Direction
A1	Coax - male	SMA Male	70MHz In	70MHz/Input
A2	Coax - male	SMA Male	70MHz Out1	70MHz/Output
A3	Coax - male	SMA Male	70MHz Out2	70MHz/Output
1	Solder Cup	BNC Female	TLM Out2	0-7.5Vp-p Analog/Out
2	Solder Cup	BNC Female	TLM Out1	0-7.5Vp-p Analog/Out
3	Solder Cup	BNC Female	AM Out	0-7.5Vp-p Analog/Out
4	Solder Cup	BNC Female	Auxiliary TTL	TTL/Input or Output
5	Solder Cup	BNC Female	Auxiliary AM	TTL or Analog AM/Out
6	Solder Cup	BNC Female	RSSI Out	0-4Vp-p Analog/Out
7-10	Solder Cup	-	-	Gnd

LS-25-D

D-connector Pin/Contact No.	D-connector Pin/Contact Type	Pigtail Type	Pigtail Label	Signal Level/ Direction
A1	Coax - male	SMA Male	70MHz Out3	70MHz/Output
A2	Coax - male	SMA Male	70MHz Out2	70MHz/Output
A3	Coax - male	SMA Male	70MHz Out1	70MHz/Output
1	Solder Cup	-	-	-
2	Solder Cup	-	-	-
3	Solder Cup	BNC Female	AM Out	0-7.5Vp-p Analog/Out
4	Solder Cup	BNC Female	Auxillary TTL	TTL/In or Out
5	Solder Cup	BNC Female	Auxillary AM	TTL or Analog AM/Out
6	Solder Cup	BNC Female	RSSI Out	0-4Vp-p Analog/Out
7-10	Solder Cup	-	-	Gnd

Figure 3-6 LS-25 / LS-25-D Pigtail connectors

4 Operation of the LS-25-D and LS-25 With The LDPS Software

The version 2 Lumistar LS-25-D Multi-band RF Downconverter and the LS-25 Multi-band FM Receiver can be setup and controlled by using the Lumistar Data Processing System (LDPS) software (shown below). A stand-alone application is also provided[2].

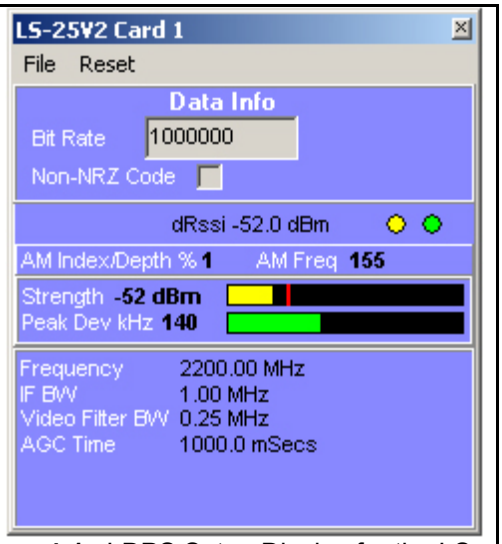


Figure 4-1 LDPS Setup Display for the LS-25-D/LS-25

The LDPS is composed of two major application programs - the Server and the Client. The Server program is used to setup and acquire data from various sources (such as the LS-25-D/LS-25). The server formats the data into a normalized format, archives it, and then pass the data on to the client application for further processing and/or display. The Client is mainly a data processing and presentation program, with hooks to allow new display and processing routines to be added by the user. The server and client applications can run together on the same computing platform, or on different platforms interconnected via a Local Area Network (LAN). This user's manual will focus primarily on the server side application.

To initially configure the LS-25-D/LS-25, perform the following steps:

1. Run the LDPS server program and from the System menu shown below, select "Devices" and then "Manage" *(System→ Devices→ Manage)*
2. From the System Manager shown in Figure 4-2 below left, select the "Enable" check box next to the LS25V2 button. The "Ls25V2_8x" button will then become active (not grayed out). Note the red rectangle around the button - this indicates that the application has not yet started. Note also the "Sim" check box next to the "Enable" check box. Checking this box allows the LDPS application to operate when a LS-25 board is not installed in the system.
3. From the System Manager, click the "Ls25V2_8x" button. This will launch the "Ls25V2_8x (Receiver)" display shown in Figure 4-2 below right. Note that the red rectangle around the button has changed to green indicating that the application is now running.
4. To setup and configure the LS-25-D and LS-25 cards, follow the procedures outlined in paragraphs 4.1.

[2] Located in the LDPS directory, the standalone application, LS25V2_8x performs the same functions as described in this section.

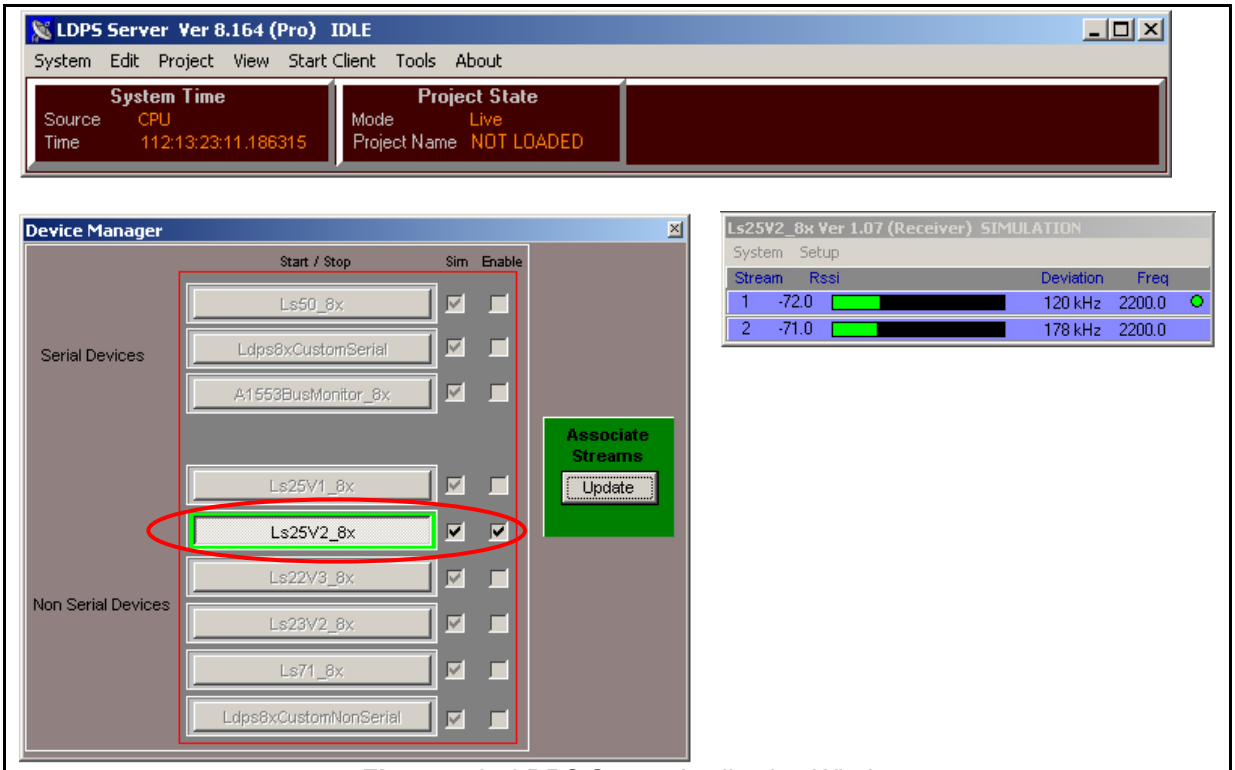


Figure 4-2 LDPS Server Application Windows

4.1 Configuring the LS-25-D/LS-25 Hardware

From the "Ls25V2_8x (Receiver)" display shown below upper left in Figure 4-3, click "Setup" and then "Stream 1" *(Setup →Stream 1).*

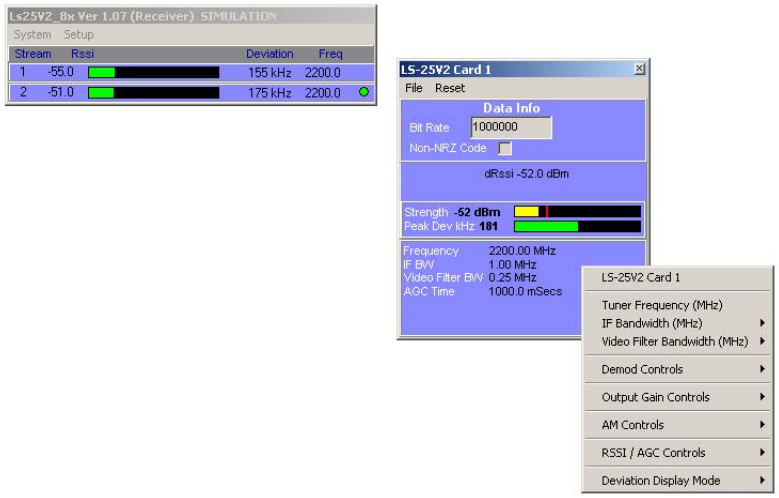


Figure 4-3 LDPS Configuration Menus/Controls for the LS-25-D/LS-25

The "LS-25V2 Card 1" display shown center in Figure 4-3 above is divided into several regions. The number of, and function of each region is dependent on the various modes the cards can be configured for.

To invoke the controls for the display, simply place the mouse curser in the center region and right click. The resulting menus are shown in Figure 4-4 below are discussed in detail in the following paragraphs.

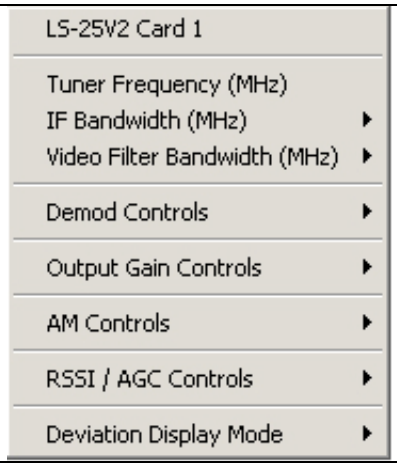


Figure 4-4 The LS-25-D/LS-25 Configuration Menu

4.1.1 Tuner Frequency

The Version 2 Lumistar LS-25-D Multi-band RF Downconverter and the LS-25 Multi-band FM Receiver concurrently support AM & FM demodulation in three the following five possible frequency bands. *Note that up to three (3) of these bands may be specified at the time of order.*

2185.5 - 2485.5 MHz (NATO E-Band)
2200.5 - 2399.5 MHz (S-Band)
1710.5 - 1849.5 MHz (Upper L-Band)
1435.5 - 1539.5 MHz (Lower L-Band)
215.5 - 319.5 MHz (P-Band)

To select a receive frequency, click on the *"Tuner Frequency (MHz)"* menu item. Enter the frequency in the pop-up dialog box shown in Figure 4-5 below left and click OK. The updated frequency will be displayed as shown in Figure 4-5 below right (red oval). Note that the supported tuner resolution is 50 KHz, and that entered values will be rounded off the nearest 50 KHz value in the display. Frequency values outside of the ranges specified above will result in an error message with no change in frequency (the default frequency is 2200.00 MHz).

Also note that the user may enter the data stream bit rate in bits/second and indicate if the stream encoding is non-NRZ (bi-phase, miller, etc.) as shown in the yellow oval in the figure below.

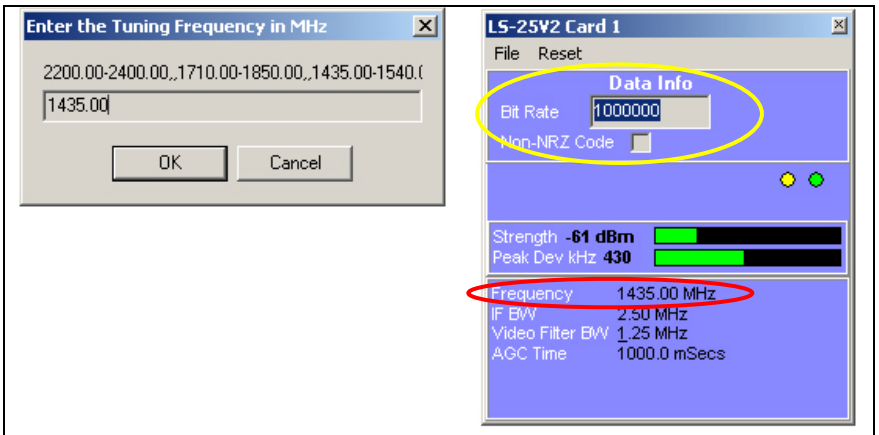


Figure 4-5 Tuning Frequency Display

4.1.2 IF Bandwidth

The Version 2 Lumistar LS-25-D Multi-band RF Downconverter and the LS-25 Multi-band FM Receiver are factory configured to support up to twelve (12) separate 2nd IF bandwidths. Standard bandwidths include: 500kHz, 1MHz, 1.5MHz, 2.5MHz, 3.5MHz, 4MHz, 6MHz, 8MHz, 10MHz, 12MHz, 16MHz, and 20MHz. At the factory the selected 2nd IF bandwidth values are programmed into a configuration PROM (see paragraph 5.2.6 on page 39 for more details) and are used by the LDPS application to populate frequency values in the pop-up list box shown in Figure 4-6 below left. In the example shown, the unit is factory configured with 2nd IF bandwidths of 1, 2.5, 5, and 10 MHz. The actual 2nd IF bandwidths the individual user will see when setting the IF bandwidth are likely to be different than those show here. Once selected, the 2nd IF bandwidth will be displayed as shown in the figure below right (red oval).

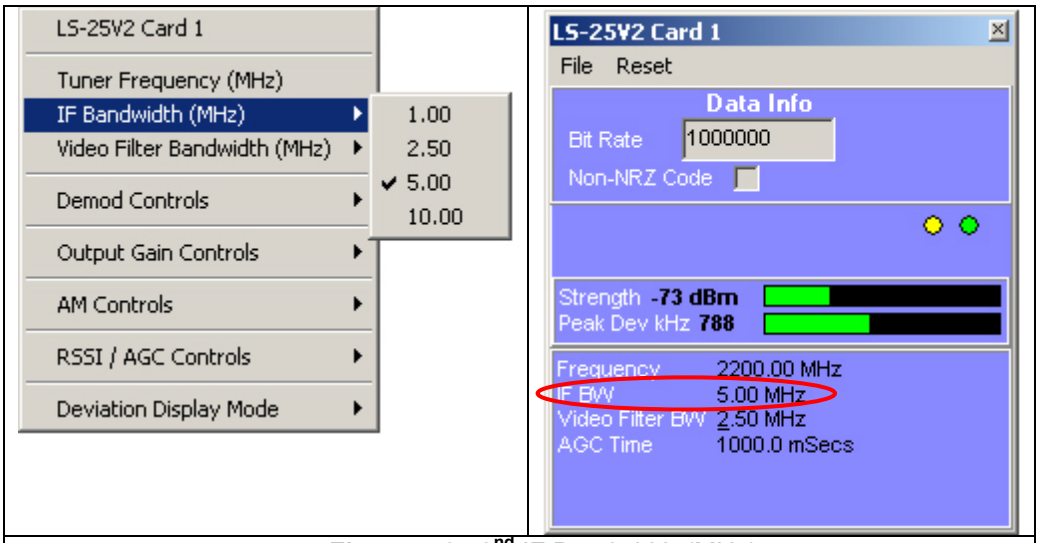


Figure 4-6 2nd IF Bandwidth (MHz)

4.1.3 Video Filter Bandwidth

The Version 2 Lumistar LS-25-D Multi-band RF Downconverter and the LS-25 Multi-band FM Receiver are factory configured to support up to twelve (12) separate Video Filter bandwidths. Standard bandwidths include: 250kHz, 500kHz, 750kHz, 1.25MHz, 1.75MHz, 2MHz, 3MHz, 4MHz, 5MHz, 6MHz, 8MHz, and 10MHz. At the factory the selected Video Filter bandwidth values are programmed into a configuration PROM (see paragraph 5.2.7 on page 39 for more details) and are used by the LDPS application to populate frequency values in the pop-up list box shown in Figure 4-7 below left. In the example shown, the unit is factory configured with Video Filter bandwidths of 0.25, 1.25, 2.50, and 5 MHz. The actual Video Filter bandwidths the individual user will see when setting the Video Filter bandwidth are likely to be different than those show here. Once selected, the Video Filter bandwidth will be displayed as shown in the figure below right (red oval).

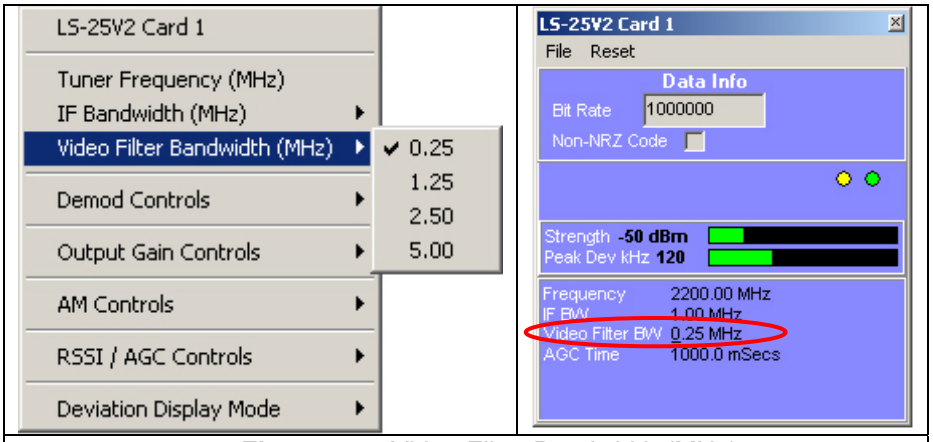


Figure 4-7 Video Filter Bandwidth (MHz)

4.1.4 Demodulation Control

The LS-25V2 Demodulation Control has three sub-modes: "External Demod Source", "AC Couple TLM2", and "Data Polarity Inverted' as shown in Figure 4-8 below.

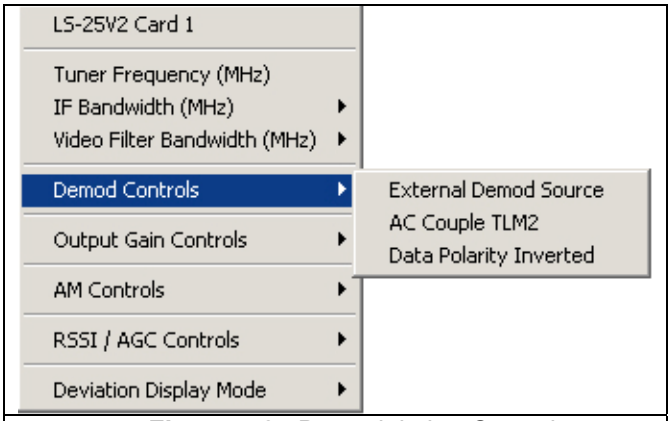
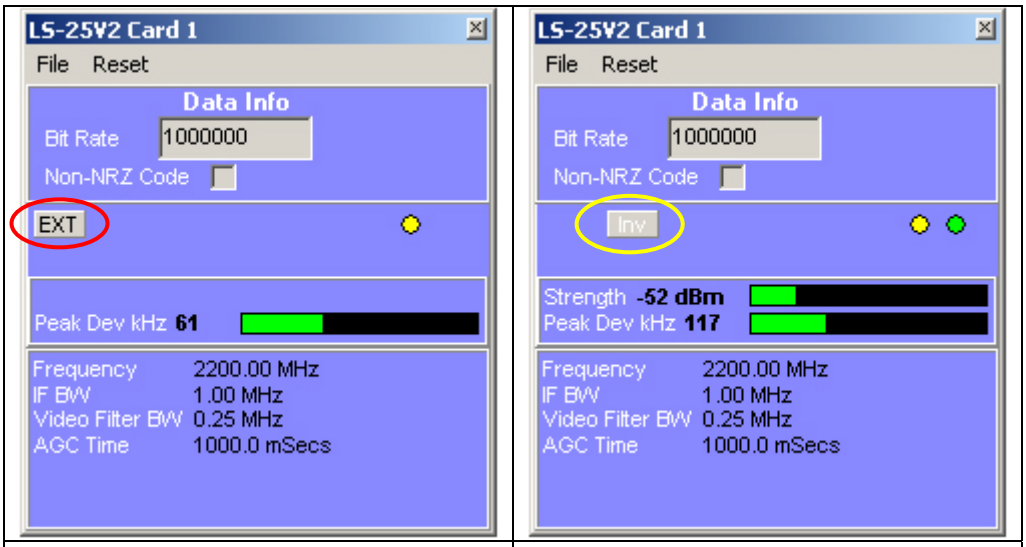


Figure 4-8 Demodulation Controls

The "External Demod Source" sub-mode enables the LS-25 FM Discriminator and Video Filter to be driven by an external input source. See paragraph 5.2.10 on page 41 for more details. The selection of this sub-mode is indicated in the display as shown in Figure 4-9 below left (red oval).



"External Demod Source"	***"Data Polarity Inverted"***

Figure 4-9 Demodulation Controls & Resulting Displays

The "AC Couple TLM2" sub-mode allows the user to select the AC coupling configuration for the TLM2 output. If this sub-mode is not selected (no check mark in the menu), then the coupling mode for the TLM2 output will default to DC coupling. See paragraph 5.2.12 on page 42 for more details.

The "Data Polarity Inverted" sub-mode allows the user to invert the logic polarity of the PCM data output. See paragraph 5.2.11 on page 42 for more details. The selection of this sub-mode is indicated in the display as shown in Figure 4-9 above right (yellow oval).

4.1.5 Output Gain Controls

The LS-25V2 Output Gain Control has two sub-modes: "Auto", and "Manual" as shown in Figure 4-10 below left. When the "Manual" sub-mode is selected, two additional slider controls will appear on the display as shown below right (red oval). The "AM Output Level" slider control allows the user to manually alter the output voltage level of the AM output on the LS-25V2. See paragraph 5.2.17 on page 46 for more details. The "TLM Output Level" slider control allows the user to manually alter the output voltage level of the TLM1 and TLM2 output signals produced by the LS-25V2. See paragraph 5.2.13 on page 43 for more details. In either case, no additional feedback is provided in the display as the sliders are adjusted. The actual voltage levels of the AM and TLM signals will need to be measured via some form of external instrumentation (volt meter, oscilloscope, etc) as each slider is adjusted.

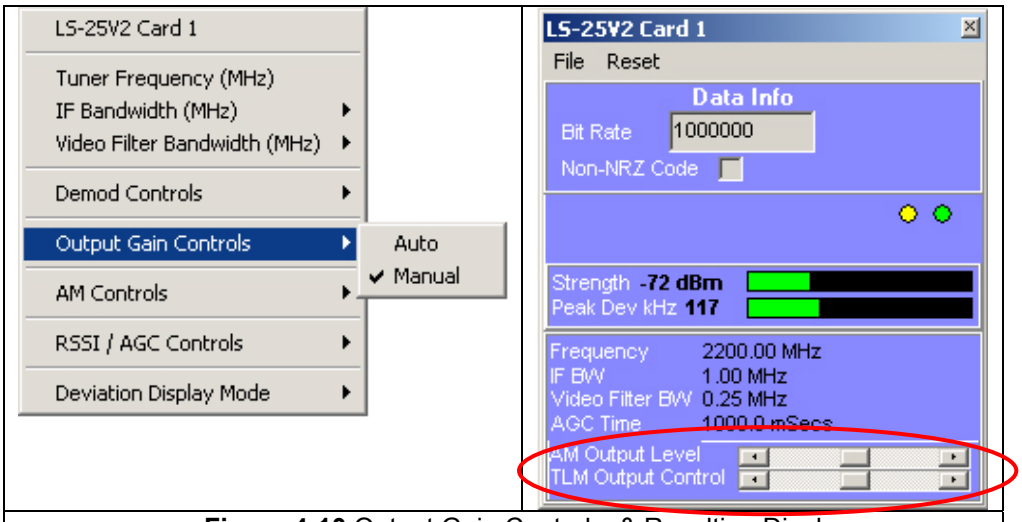


Figure 4-10 Output Gain Controls & Resulting Display

4.1.6 AM Controls

The LS-25V2 AM Controls has two sub-modes: "AM Low Pass Filter (Hz)", and "View AM Data" as shown in Figure 4-11 below left. When the "View AM Data" sub-mode is selected, two additional data displays will appear on the display as shown below right (red oval). The "AM Index Depth%" is the amplitude modulation index detected in the post-processing of the AM demodulation. See paragraph 5.2.14 on page 44 for more details. The "AM Freq" is the instantaneous frequency value of the AM demodulated signal (Hz). See paragraph 5.2.16 on page 45 for more details.

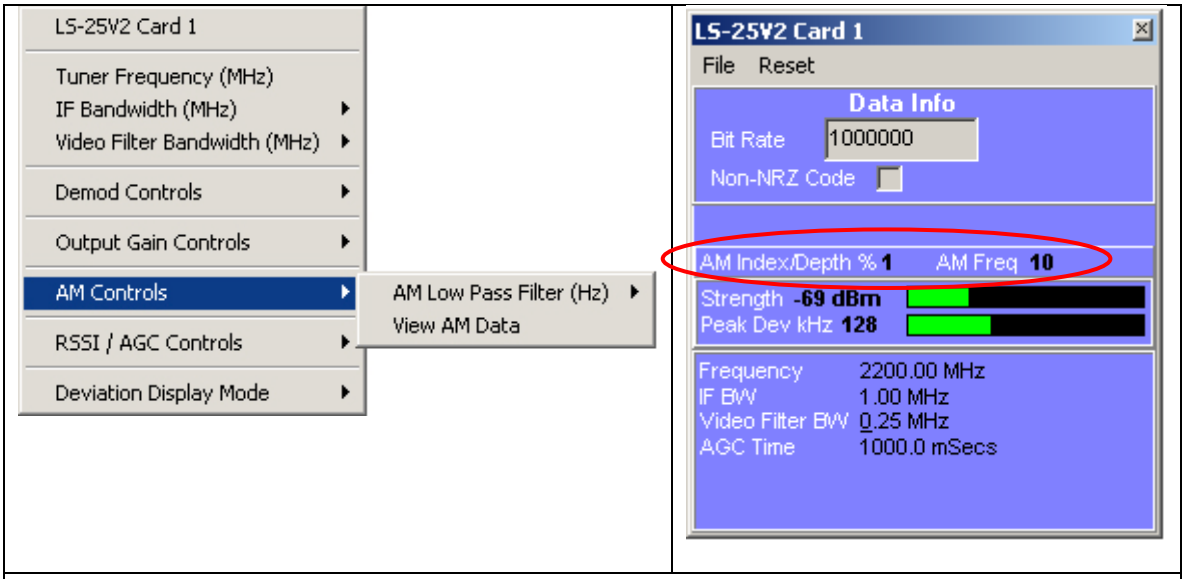


Figure 4-11 AM Controls

The "AM Low Pass Filter (Hz)" sub-mode allows the user to select one of four low-pass filters on the AM output including; 50, 500, 5000, or 50,000 Hz. Note, the 50 KHz selection is the same as low-pass filter bypass. See paragraph 5.2.15 on page 44 for more details.

4.1.7 RSSI/AGC Controls

The LS-25V2 RSSI/AGC Control has three sub-modes: "AGC Time Constant", "Delta RSSI Mode", and "Set Delta RSSI Point" as shown in Figure 4-12 below left. The "AGC Time Constant" sub-mode allows the user to select one of four possible AGC time constants including; 33, 100, 330, and 1000 ms. The selected time constant is displayed as shown in Figure 4-12 below right (yellow oval). For more information on Automatic Gain Control (AGC) time constants, see paragraph 5.2.18 on page 48.

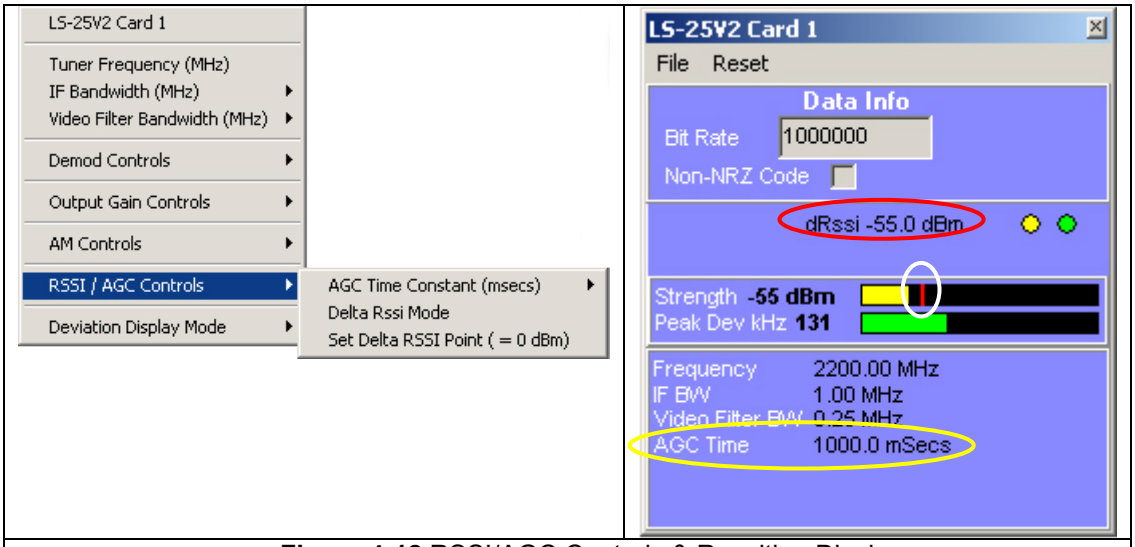


Figure 4-12 RSSI/AGC Controls & Resulting Display

The "Delta RSSI Mode", and "Set Delta RSSI Point" sub-modes are used in concert with each other. The "Set Delta RSSI Point" sub-mode initiates the acquisition of the instantaneous RF input power (dB) or signal strength level at the input to connector J2. This *snapshot* captures and establishes an absolute input power reference level that is subsequently compared continuously with the instantaneous RF input power level. The difference, or delta between the reference and instantaneous levels is displayed in two ways as shown in Figure 4-12 above right. The numerical value of the delta is shown as indicated by the red oval. The reference level is represented by a vertical red line shown in the white oval portion of the signal strength bar graph. For more information on the Received Signal Strength Indication (RSSI), see paragraph 5.2.8 on page 40.

4.1.8 Deviation Display Modes

The LS-25V2 Deviation Display Mode Control has three sub-modes: "IF BW Percentage", "Approx FM Deviation", and "None" as shown in Figure 4-13 below left. The "None" mode display is shown in Figure 4-13 below right.

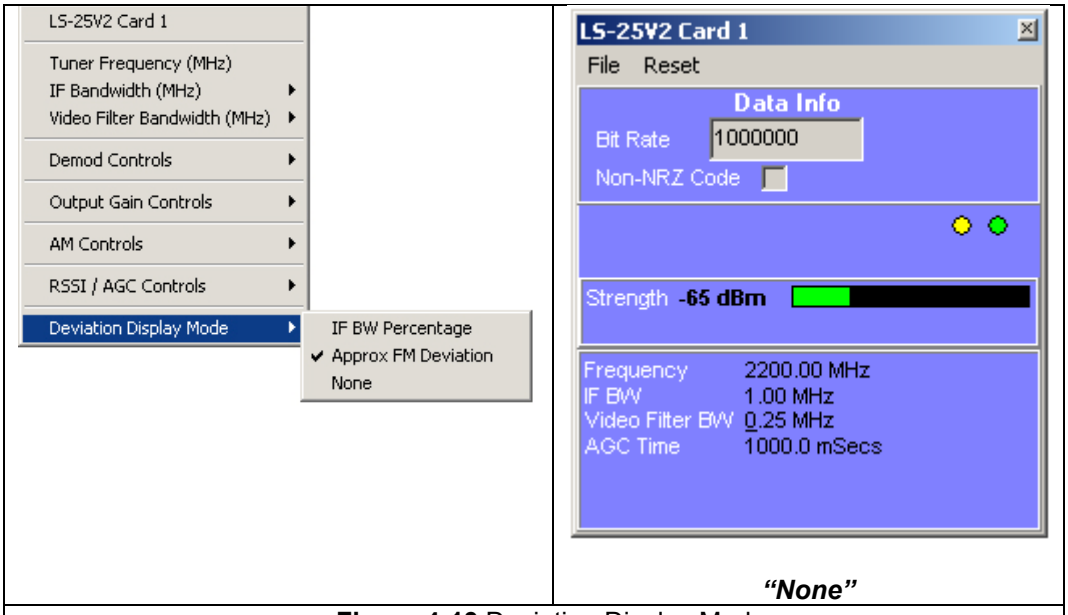


Figure 4-13 Deviation Display Modes

The "Approx FM Deviation" sub-mode is shown in Figure 4-14 below right and indicates the peak FM deviation of the signal (red oval). The "IF BW Percentage" sub-mode is shown in Figure 4-14 below left and indicates the deviation percentage of the signal (yellow oval). For more information the FM deviation status, see paragraph 5.2.9 on page 40.

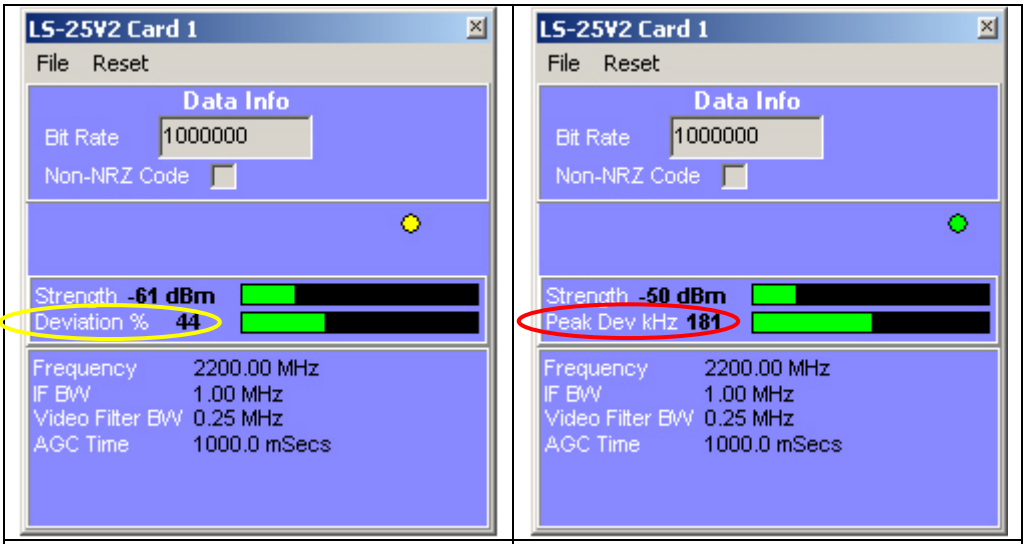


Figure 4-14 Additional Deviation Displays

5 Programming

This chapter provides receiver software interface and setup information. Depending on the form factor ordered, the receivers provide command and status interfaces through either a 32-bit Peripheral Component Interface bus (PCI version 2.2) or an 8-bit Industry Standard Architecture bus (ISA). Both interfaces use the same command formatting and command/status register sets.

5.1 Bus Interfaces

The receiver is controlled by an array of eight registers. Each register is eight bits in length. Depending on the physical bus structure connecting the receiver to the system, the register number will map to a machine address in various ways.

5.1.1 PCI Bus Interfaces

PCI components do not have fixed address assignments. At system startup, a power-on routine scans the computer for PCI interfaces and assigns system resources to the devices found.

Each PCI component is assigned an array of sixty-four 32-bit registers in what is referred to as configuration space. This area is normally not accessible anywhere in system address space and must be accessed by special means that are system-dependent.

The following discussion applies to systems using *MS–DOS* or Microsoft *Windows* platforms where PCI configuration space is accessed by BIOS calls. For the purposes of this document, these environments will be referred to as "typical" operating system environments. Other environments will have system-specific ways to access PCI configuration space. If you are utilizing non-Microsoft operating systems, consult your operating system documentation to determine PCI access methods. In addition, for environments that utilize processing platforms other than X86-type processors, Big/Little-Endian data format issues may also be present.

To locate a receiver in a typical operating system environment, the following steps are required:

1.) Initialize an "*index*" value to zero. This index is allowed to be as large as 255 by the PCI specification.

2.) To locate the boards PCI9080 interface, set the machine registers as follows:

```
AX = 0xB102
CX = 0x9080
DX = 0x10B5
SI = index
```

3.) Issue a software interrupt (0x1A). If the system returns from the interrupt with the carry flag set, any such devices are already located and no (more) exist. Exit the scanning routine. If the carry flag is clear, the BIOS call will have returned a "*handle*" in the BX register.

4.) If the carry flag was clear, read the sub-identifier. Set the registers as follows:

AX = 0xB10A
BX = *handle*
SI = 0x2C

5.) Issue another software interrupt (0x1A). The interrupt returns a value in the ECX register. If the value returned is 0x1B16B00B, the handle points to a receiver and other configuration registers may be accessed. (Otherwise skip to step 7.) Set registers as follows:

AX = 0xB10A
BX = *handle*
SI = 0x1C

6.) Issue another software interrupt (0x1A). Logically AND the value returned in the ECX register with 0x0FFF0. This yields the base I/O port of the receiver. Registers are in PCI I/O space and map simply as:

Register Address = Base I/O Port + Register Address Offset

7.) Increment the index value and return to step 5.

5.1.2 ISA Bus Interfaces

For ISA Receivers, the address of the Base I/O Port is selected by the user via switch SW4. (See Figure 3-3 on page 16 for details). In ISA bus systems, care should be taken to ensure that the I/O range selected is free for receiver operations. Once a free register range has been identified and the corresponding switch selections have been made, board registers are in ISA I/O space and map simply as:

Register Address = Base I/O Port + Register Address Offset

5.2 Command and Status Registers

Table 5-1 below contains the map for the receiver command and status registers. Register address offsets are indicated in this table. More detailed discussions of the function and interaction of these registers will follow in subsequent sections. Discussions will follow a logical and functional flow rather than on a register-by-register method.

Command Registers								
Mnemonic	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CMD0	TLM2 Output Coupling	FM Demod Data Polarity	FM Demod Input Source	Accessory Controls		Linear Out	AGC Time Constant Select	
CMD1	*(Unused)*				Board LED ID3	Board LED ID2	Board LED ID1	Board LED ID0
CMD2	Video Filter Select				IF Filter Select			
CMD3	*Reserved* (Logic "1")	Operational Mode Controls			AM Output Filter Select		RF Band Select	
CMD4	Mode Register 1 (MDR1)							
CMD5	Mode Register 2 (MDR2)							
CMD6	Mode Register 3 (MDR3)							
CMD7	Digipot Command Enable	*(Unused)*					Digipot Mode Select	

Status Registers								
Mnemonic	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
STAT0	*Reserved* (Logic "0")	Board Identification Register						
STAT1	RSSI Status Bit 1	RSSI Status Bit 0	*(Unused)*		Board LED ID3 Status	Board LED ID2 Status	Board LED ID1 Status	Board LED ID0 Status
STAT2	AM Index/Depth Status							
STAT3	Receiver BUSY Flag	Operational Mode Status			Auto Store Status	Diversity Lock Status	AM Freq Counter Update	AM Freq Counter Overflow
STAT4	Received Signal Strength Indication (RSSI) Status (Bits 9-2)							
STAT5	FM Deviation Status							
STAT6	Status Register 1 (STAT1)							
STAT7	Status Register 2 (STAT2)							

Table 5-1 Receiver Command and Status Register Table

5.2.1 General Communications Interaction

Communications with the receiver is via a command-response format. Commands sent from the host processor will cause a BUSY flag to be set in bit 7 of *Status Register 3*. Once a command has been issued, application software should wait until the BUSY flag resumes a low state prior to issuing further commands or reading the requested status data. Figure 5-1 below illustrates the BUSY flag.

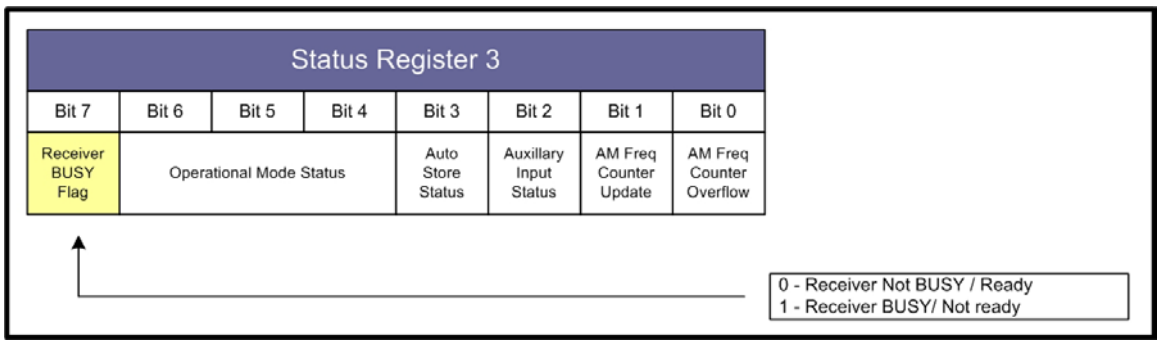


Figure 5-1 Receiver BUSY Flag Indication

5.2.2 Hardware Identification

The receiver contains a hardware identification register to allow software the ability to query the hardware to provide confidence that a receiver is physically present at the alleged address. This register is shown in Figure 5-2 below.

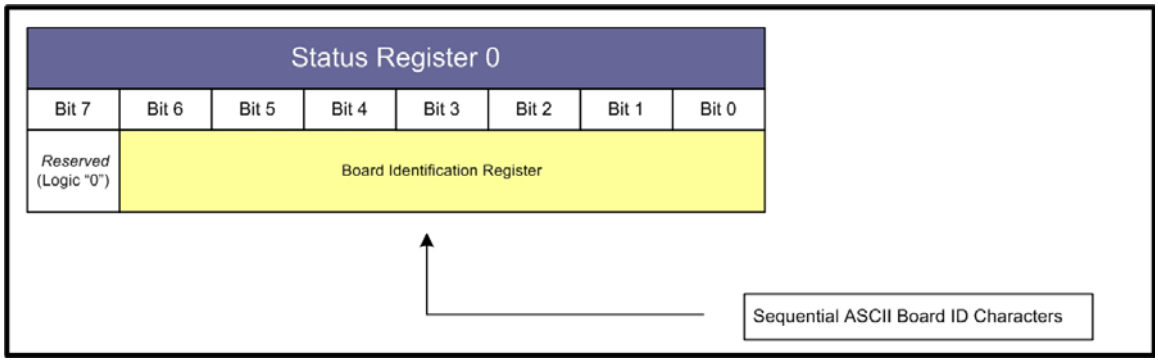


Figure 5-2 Board Identification

Successive reads from the *Status Register 0* will return a string of ASCII characters in the lower 7 bit positions of the register as follows:

Receiver Type:	Hex Return String:	ASCII Return String:
LS-25	0x4C, 0x53, 0x32, 0x35, 0x56, 0x32, 0x00	"L", "S", "2", "5", "V", "2", "*NULL*"
LS-25-D	0x4C, 0x53, 0x32, 0x31, 0x56, 0x32, 0x00	"L", "S", "2", "1", "V", "2", "*NULL*"

This receiver presents these identification strings in a circular fashion terminating in a *NULL* character (0x00). Once the *NULL* character is received, subsequent reads from this register will recycle through the character string.

5.2.3 LED Control

The rear of the PCI and ISA receiver designs contains a bank of four Board ID LEDs. At initial application of power, the DSP maintains control of these indicators. The DSP utilizes the LEDs to indicate power-up test and configuration memory load status. During this phase of operation, two LED cycles occur. The first cycle flashes the four LEDs in groups of two indicating that the DSP processor has passed its initial built-in-test cycle. The second cycle illuminates each of the LEDs in a binary sequence indicating successful loads of configuration memory pages. The internal control of these LEDs is complete in less than 3 seconds. After the final configuration page has been loaded, all LEDs are extinguished and control is returned to bits 0 through 3 of *Command Register 1*. Status of these LEDs can be read by the application software via bits 0 through 3 of *Status Register 1*. Figure 5-3 illustrates registers used to command and status the boards LEDs.

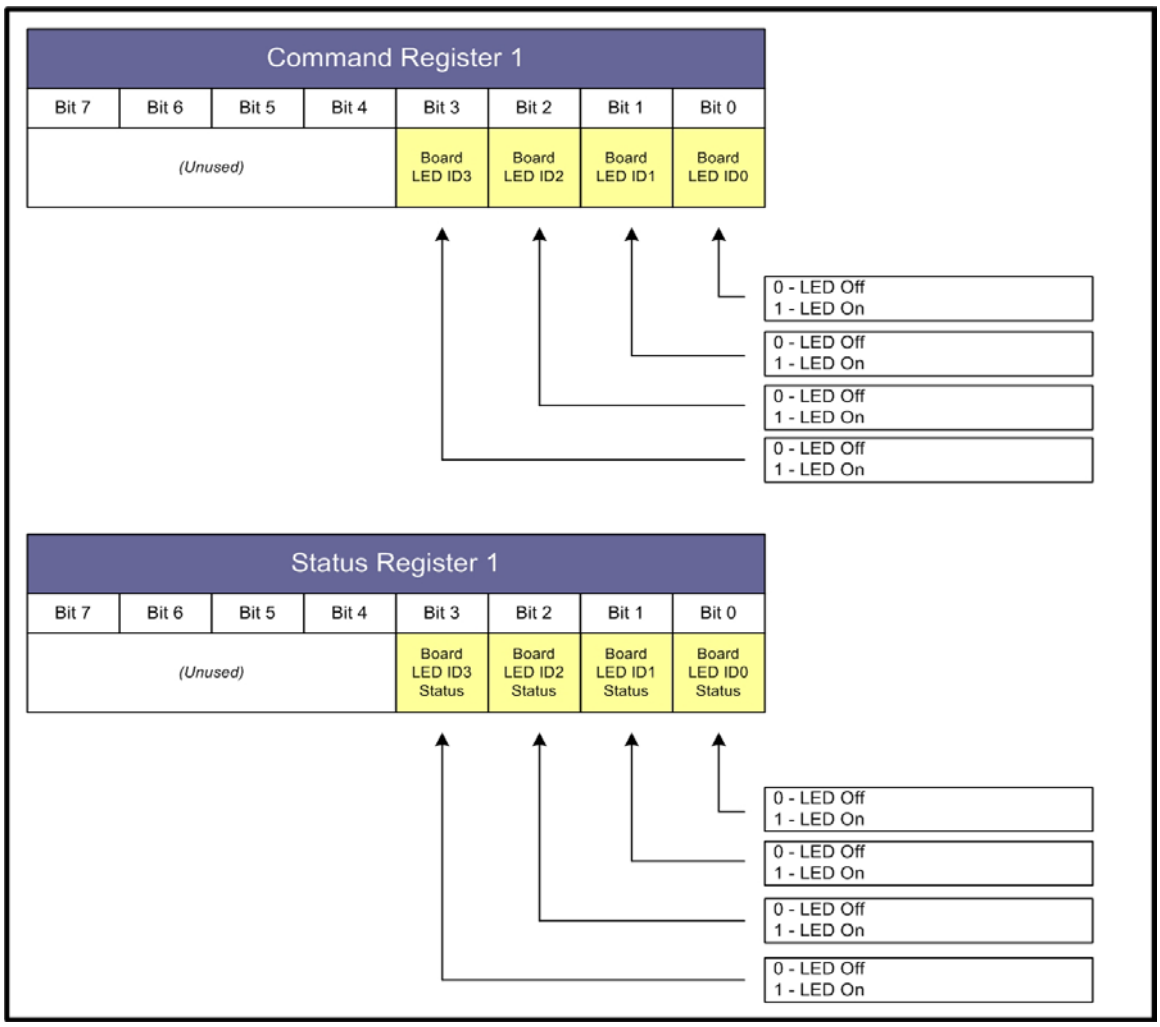


Figure 5-3 LED Control and Status

Information:

LED indications during power-up phases provide a source of general receiver health and operational status.

One application for these LEDs is as a means for the device driver or software application to provide receiver identification when multiple instances of a physical device are present in a system.

5.2.4 Configuration Data

The receiver provides the application software with hardware configuration information detailing available filters and hardware status. This data is held internally in the receiver in a configuration PROM. The contents of this configuration PROM are contained in Table 5-2 below.

PROM Address Offset (Hex)	PROM Address Offset (Dec)	Register Contents
0x00	**0**	IF Filter 0 Bandwidth (kHz)
0x01	**1**	IF Filter 1 Bandwidth (kHz)
0x02	**2**	IF Filter 2 Bandwidth (kHz)
0x03	**3**	IF Filter 3 Bandwidth (kHz)
0x04	**4**	IF Filter 4 Bandwidth (kHz)
0x05	**5**	IF Filter 5 Bandwidth (kHz)
0x06	**6**	IF Filter 6 Bandwidth (kHz)
0x07	**7**	IF Filter 7 Bandwidth (kHz)
0x08	**8**	IF Filter 8 Bandwidth (kHz)
0x09	**9**	IF Filter 9 Bandwidth (kHz)
0x0A	**10**	IF Filter 10 Bandwidth (kHz)
0x0B	**11**	IF Filter 11 Bandwidth (kHz)
0x0C	**12**	Video Filter 0 Bandwidth (kHz)
0x0D	**13**	Video Filter 1 Bandwidth (kHz)
0x0E	**14**	Video Filter 2 Bandwidth (kHz)
0x0F	**15**	Video Filter 3 Bandwidth (kHz)
0x10	**16**	Video Filter 4 Bandwidth (kHz)
0x11	**17**	Video Filter 5 Bandwidth (kHz)
0x12	**18**	Video Filter 6 Bandwidth (kHz)
0x13	**19**	Video Filter 7 Bandwidth (kHz)
0x14	**20**	Video Filter 8 Bandwidth (kHz)
0x15	**21**	Video Filter 9 Bandwidth (kHz)
0x16	**22**	Video Filter 10 Bandwidth (kHz)
0x17	**23**	Video Filter 11 Bandwidth (kHz)
0x18	**24**	*(Unused)*
0x19	**25**	*(Unused)*
0x1A	**26**	RF Band 0 Lower Band Limit (MHz)
0x1B	**27**	RF Band 0 Upper Band Limit (MHz)
0x1C	**28**	RF Band 1 Lower Band Limit (MHz)
0x1D	**29**	RF Band 1 Upper Band Limit (MHz)
0x1E	**30**	RF Band 2 Lower Band Limit (MHz)
0x1F	**31**	RF Band 2 Upper Band Limit (MHz)
0x20	**32**	*(Unused)*
0x21	**33**	*(Unused)*
0x22	**34**	RF Band 0 RSSI 1st Order Poly (Mx+B): M Scale Factor x 1000
0x23	**35**	RF Band 0 RSSI 1st Order Poly (Mx+B): B Scale Factor x 10
0x24	**36**	RF Band 1 RSSI 1st Order Poly (Mx+B): M Scale Factor x 1000
0x25	**37**	RF Band 1 RSSI 1st Order Poly (Mx+B): B Scale Factor x 10
0x26	**38**	RF Band 2 RSSI 1st Order Poly (Mx+B): M Scale Factor x 1000
0x27	**39**	RF Band 2 RSSI 1st Order Poly (Mx+B): B Scale Factor x 10
0x28	**40**	*(Unused)*
0x29	**41**	*(Unused)*
0x2A	**42**	RSSI Time Constant 0 (x100usec)
0x2B	**43**	RSSI Time Constant 1 (x100usec)
0x2C	**44**	RSSI Time Constant 2 (x100usec)
0x2D	**45**	RSSI Time Constant 3 (x100usec)
0x2E	**46**	DSP Firmware Version ID

Table 5-2 Configuration PROM Contents

Registers required to access the PROM data are shown in Figure 5-4 on page 37.

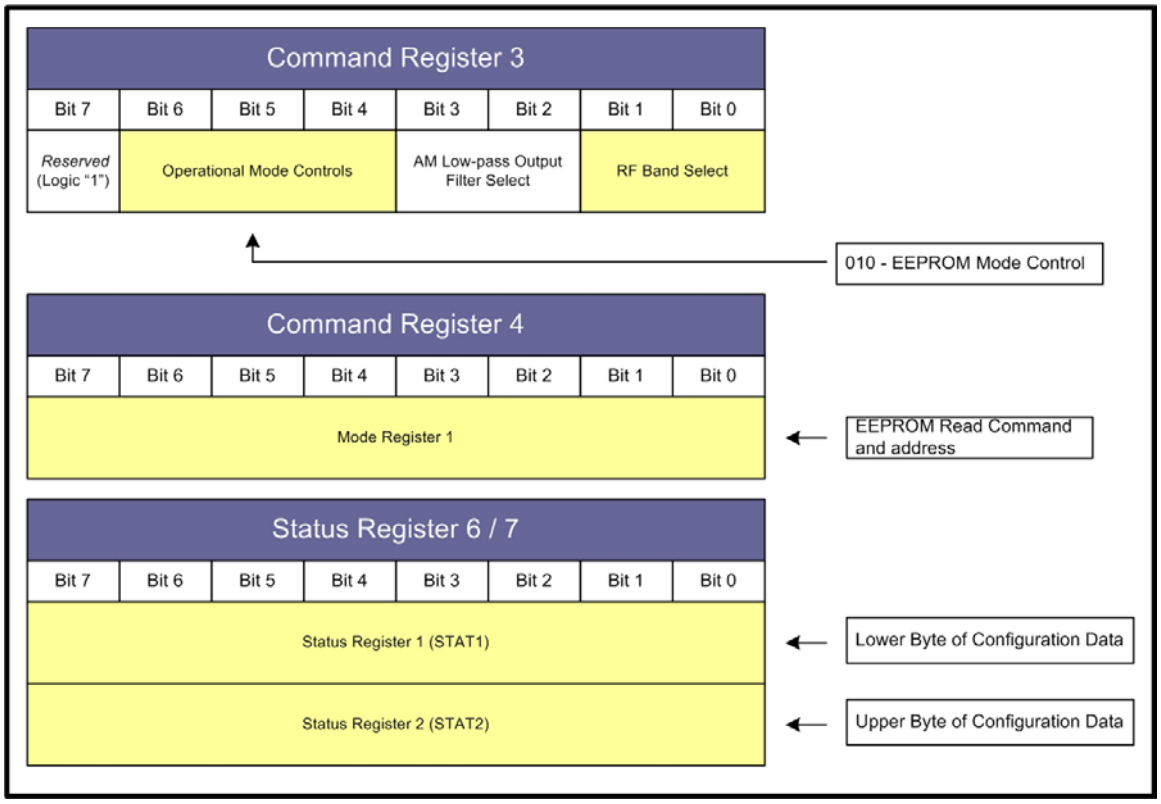


Figure 5-4 Configuration PROM Control and Status

To access the configuration data, the following steps should be performed:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Place the receiver in PROM Read mode by setting bits 6 through 4 of *Command Register 3* as follows: 010_b
3.) Poll the BUSY bit until it returns low.
4.) In *Command Register 4*, write $01aaaaaa_b$ where "*aaaaaa*" is the binary address of the desired configuration data from Table 5-2 on page 36.
5.) Once the BUSY bit goes low, the lower byte of the requested configuration data will be available in *Status Register 6*, and the upper byte of data will reside in *Status Register 7*.

Information:

It is suggested that the receiver configuration data be read as part of the application software's initialization process and held internally. Access to the EEPROM data is a slow hardware process.

5.2.5 Receiver RF Tuning

The tuning of the receiver is a two-stage process. First, the proper receiver RF input must be selected followed by the RF synthesizer tuning process. Registers that are required for tuning are depicted in Figure 5-5 below.

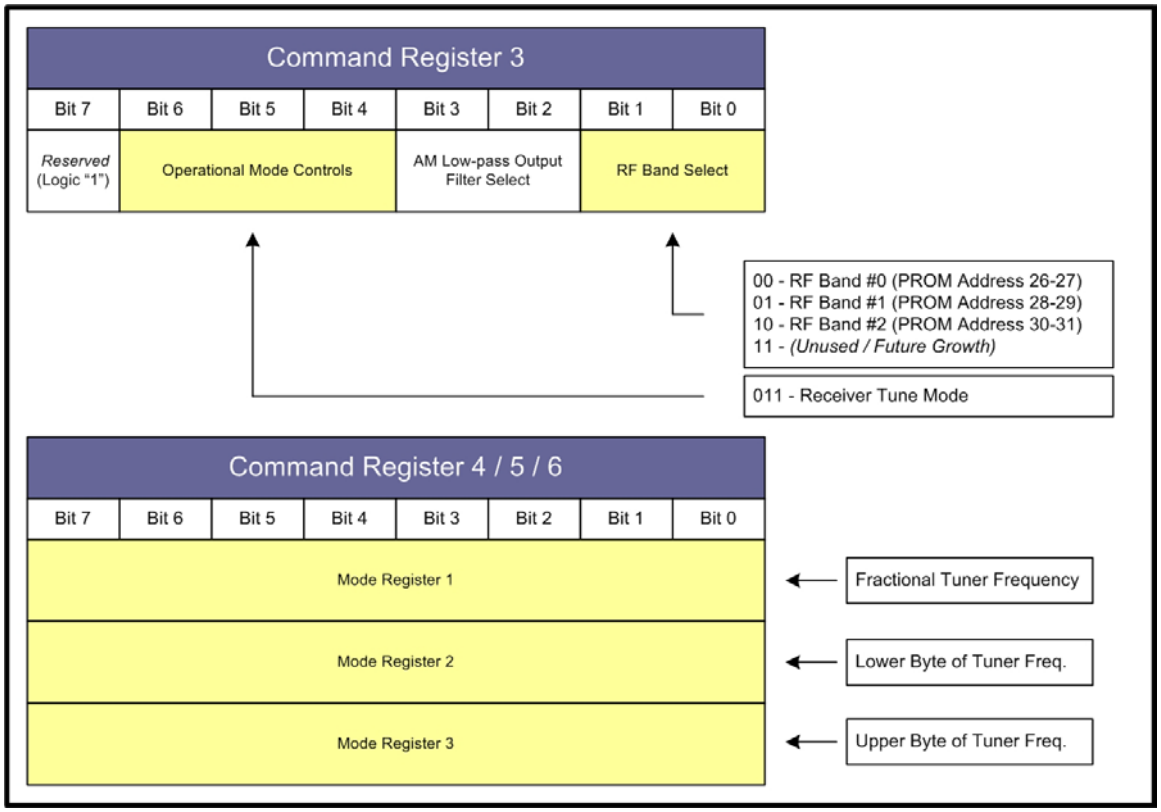


Figure 5-5 Receiver Tuning

Tuning should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Select the RF band that you desire to tune. To do this, follow the steps below:

   a. Determine which RF Band of the radio contains the desired tuning signal by comparing the programmed value with the tuning ranges from the configuration PROM. RF Band 0 band limits are contained in PROM locations 26 and 27. RF Band 1 band limits are contained in PROM locations 28 and 29. RF Band 2 band limits are contained in PROM locations 30 and 31. RF Band limits that contain 0 indicate that no RF filters are present for a given input selection and therefore, should not be selected.

   b. Once the correct band has been determined, write the corresponding band selection bits to the RF Band Select bits of *Command Register 3*.

3.) Divide the desired F_c by 256MHz, truncate the value to an integer and write the resulting value to *Command Register 6*.

4.) Perform the following calculation: (F_c modulo (256MHz))/1MHz. Truncate the value to an integer and write the resulting value to *Command Register 5.*
5.) Perform the following calculation: (F_c modulo (1MHz))/10kHz. Truncate the value to an integer and write the resulting value to *Command Register 4*
6.) Place the receiver in RF Tune mode by setting bits 6 through 4 of *Command Register 3* as follows: 011_b
7.) Once the BUSY bit goes low the tuning process is complete.

Register Example: Tune the Receiver to 2252.5MHz

CMD6 = 2252.5MHz/256MHz = 8.79 = 8
CMD5 = (2252.5MHz MOD 256MHz)/1MHz = 204.5 = 204
CMD4 = (2252.5MHz MOD 1MHz)/10kHz = 50

5.2.6 IF Filter Selection

The receiver provides for the selection of one of twelve 2nd IF filter bandwidths. The available bandwidths are indicated in the configuration PROM locations 0 through 11. If the PROM location for a particular filter contains a value of 0, this indicates that the filter is not installed and should not be selected. Figure 5-6 below contains the register contents required to select the IF filters.

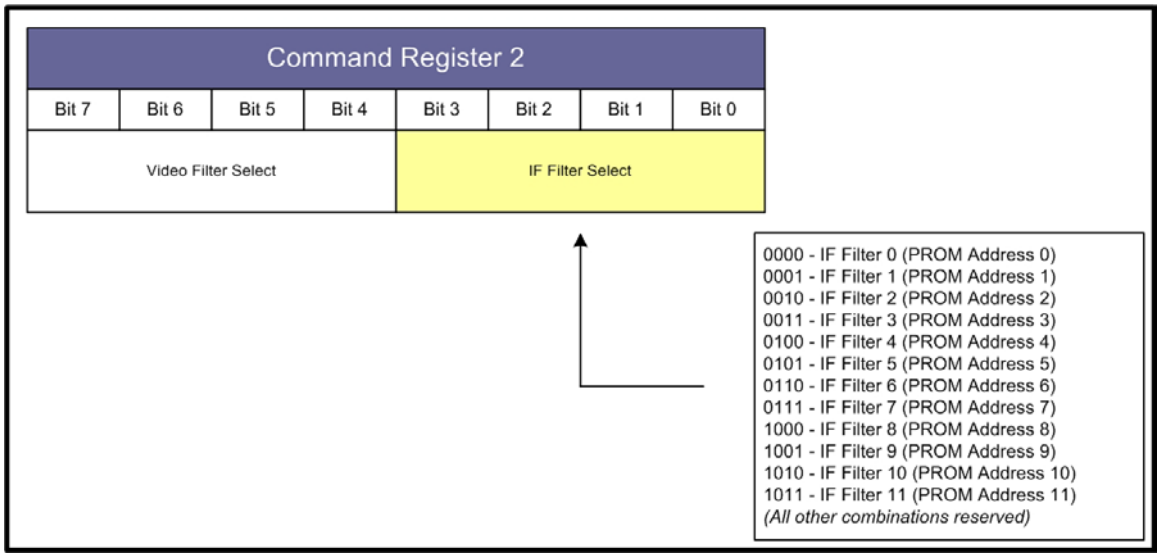


Figure 5-6 IF Filter Selection

Selection of the IF filter should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Enter the desired IF Filter number in bits 3 through 0 of *Command Register 2*.

5.2.7 Video (Post Detect) Filter Selection

The receiver provides for the selection of one of twelve of video filter bandwidth. The available bandwidths are indicated in the configuration PROM locations 12 through 23. If the PROM

location for a particular filter contains a value of 0, this indicates that the filter is not installed and should not be selected. Figure 5-7 below contains the register contents required to select the video filters.

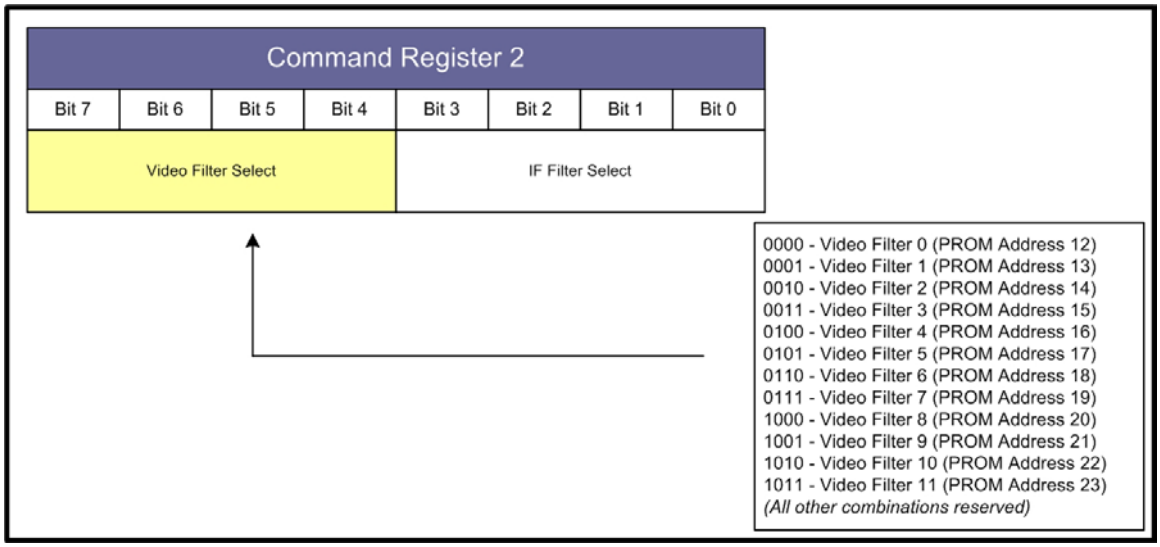


Figure 5-7 Video (Post Detect) Filter Selection

Selection of the Video filter should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Enter the desired Video Filter number in bits 7 through 4 of *Command Register 2*.

For the LS-25-D receiver, the video filter selection control bits are non-functional.

5.2.8 Received Signal Strength Indication (RSSI)

Status Register 4 provides an 8-bit indication of the RF signal strength being applied at the RF Input (J2). As signal strength increases, the value of this register increases. To obtain the signal strength in dB, the value from the register must be applied to a first order polynomial equation whose factors are contained in the configuration PROM. To calculate the RSSI value in dBm, perform the following steps:

1.) Read the value (RSSI RAW) from *Status Register 4*.
2.) Obtain the "M" and "B" values from the configuration PROM values based on which RF Band has been selected.
3.) Scale the results per the following equation:

Scaled RF Input Level (dBm) = (0.001) x (M) x (RSSI RAW) + (0.1) x (B)

5.2.9 FM Deviation Status (LS-25 ONLY)

The LS-25 version of the receiver provides the application software with a deviation reading from the output of the FM discriminator stage. With FM modulation, deviation corresponds to

modulation. However, a definition of 100% modulation is much more arbitrary and is defined case by case as the point where the transmitter frequency differs from its nominal center frequency by some specified offset. For telemetry transmission, the IRIG-106 standard suggests that peak deviation be set to 35% of the signal bit rate for NRZ signals and 70% for Bi-Phase signals.

In the receiver, a discriminator detects the FM signal, which has a gain expressed as v/ΔHz. This signal passes through the selected amplifier/post-detect filter combination to the receiver output. The gain of the amplifier is set to a value inversely proportional to the post-detect cutoff, based on the presumption that less deviation will be used for signals at lower data rates. The amplifier output is measured to provide the deviation output. The deviation value is then scaled and displayed in *Status Register 5*.

For the LS-25 receiver design, the value that is displayed in the register is a percentage of the maximum deviation value that can be carried by the selected IF bandwidth based on the IRIG standard values. The way that this is calculated is as follows:

Indicated FM Deviation % = ((Measured Deviation) / ((IF Bandwidth / 1.2) x 0.35) x 100

Nominally the deviation readout will be 100% if the signal is modulated according to standards and if the bit rate is close to the post-detect cutoff. If excess deviation is used, the value returned could exceed 100% to a maximum value of 120%. If the signal strength is small the receiver noise floor starts to intrude and will cause the deviation to falsely return a larger value than the signal characteristics would imply.

For the LS-25-D receiver, this register is non-functional.

5.2.10 FM Demodulation Input Selection (LS-25 ONLY)

The LS-25 receiver design allows the user to select the source to the dual FM discriminator stage. Either the internal 70MHz source may be used as a discriminator input or an external input via the J5 connector may be selected. Figure 5-8 below contains the selection register for the demodulator input.

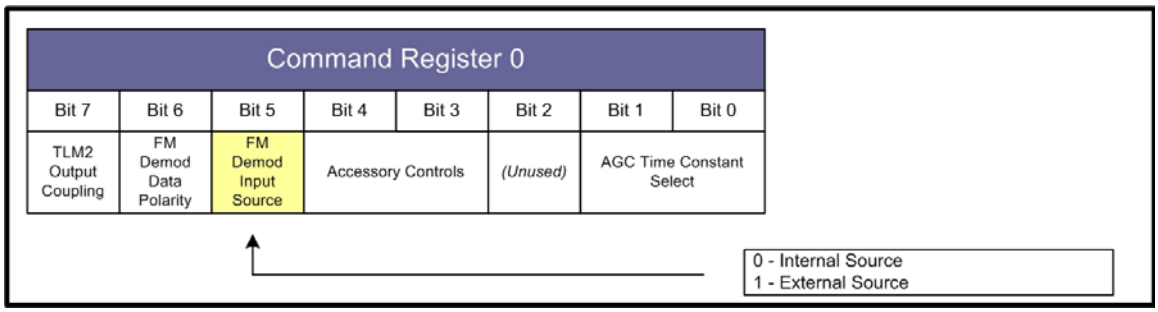


Figure 5-8 FM Demodulation Input Selection

Selection of the FM demodulator input should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Enter the desired logic state in bit 5 of *Command Register 0*.

For the LS-25-D, this control is non-functional.

5.2.11 FM Demodulation Data Polarity Selection (LS-25 ONLY)

The LS-25 receiver allows the application software to select the polarity of the PCM data output. This function may be necessary for spectrally inverted RF input sources. Figure 5-9 below contains the selection register for the PCM output data polarity.

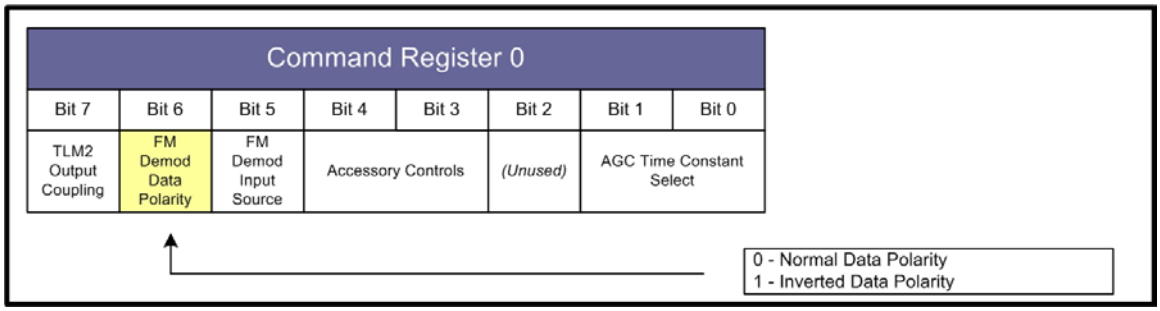


Figure 5-9 FM Demodulator Data Polarity Selection

Selection of the FM output data polarity should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Enter the desired logic state in bit 6 of *Command Register 0*.

For the LS-25-D, this control is non-functional.

5.2.12 TLM2 Output Coupling Selection (LS-25 ONLY)

The LS-25 receiver allows the application software to select the coupling of the TLM2 PCM output port. Figure 5-10 below contains the register contents required for selecting the output coupling.

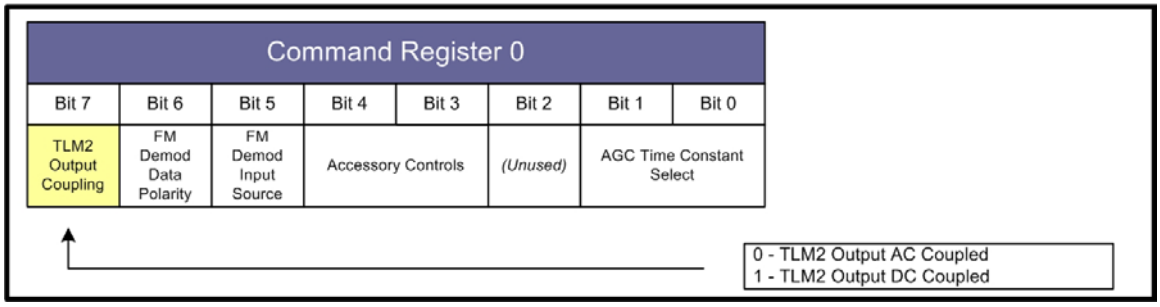


Figure 5-10 TLM2 PCM Output Coupling Selection

Selection of the TLM2 Output coupling method should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Enter the desired logic state in bit 7 of *Command Register 0*.

Information:

The TLM output coupling command only affects that TLM2 output. This command has no affect on the TLM1 output.

For the LS-25-D, this control is non-functional.

5.2.13 TLM Output Gain Controls (LS-25 ONLY)

The LS-25 receiver allows the application software to manually control the output voltage of the telemetry (TLM1 and TLM2) signal produced by the receiver. The receiver's TLM outputs are factory calibrated to produce a 4Vp-p video filter output based on 100% FM deviation for each filter selection. However, in cases where 100% of the standard deviation is not present, the user may elect to change the PCM output level. The application software is provided a 14-bit control value to adjust the PCM output level. A value of zero written to the control registers sets the output level to approximately 500mVp-p. Maximum values adjust the output level to the maximum amount for a given deviation level. Figure 5-11 below contains the register contents required for altering the PCM output levels.

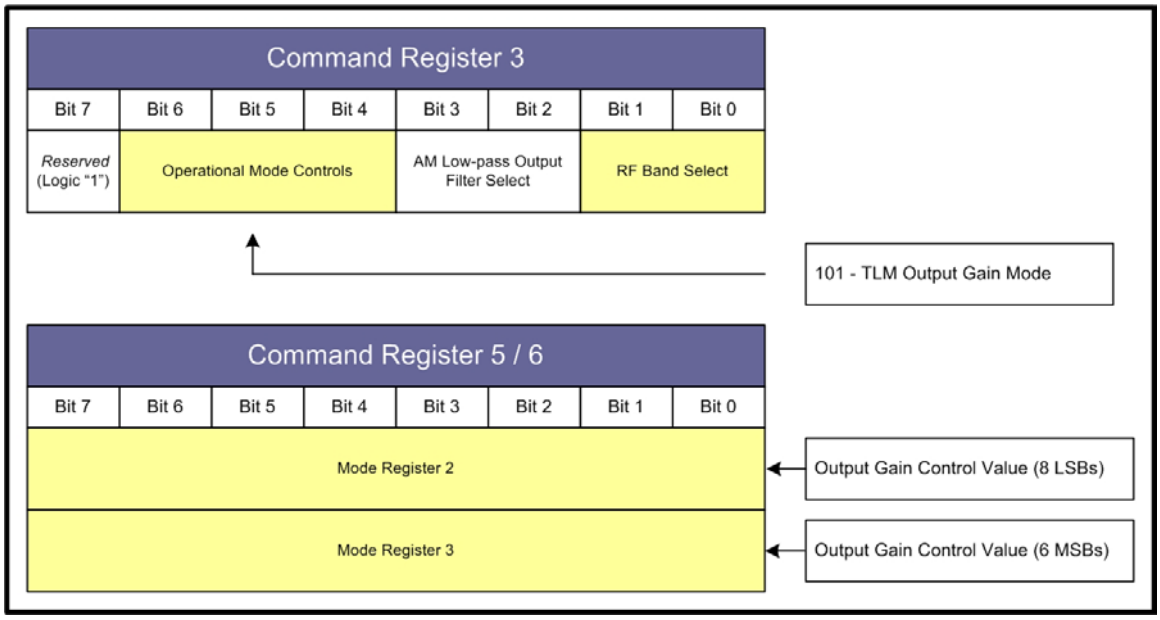


Figure 5-11 TLM Output Gain Controls

PCM output gain control adjustments should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Write the lower 8 bits of the desired output control level to *Command Register 5*.
3.) Write the upper 6 bits of the desired output control level to bits 5 through 0 of *Command Register 6.* Bits 6 and 7 of *Command Register 6* are unused.
4.) Place the receiver in PCM Output Gain Control mode by setting bits 6 through 4 of *Command Register 3* as follows: 101_b
5.) Once the BUSY bit goes low the tuning process is complete.

For the LS-25-D, this TLM Gain Control is non-functional.

5.2.14 AM Index/Depth Status

Status Register 2 contains the AM Index (or AM Depth) that has been detected in the post-processing of the AM demodulation. In AM modulation, 100% modulation is defined as the level where the negative peaks of the modulating signal reduce the transmitted signal output to zero. The values returned indicate the percentage of AM modulation detected by the receiver. These values will vary from 0 to 100, which are direct percentage relations.

It is important to note that AM Index detection is performed during all operational phases of the receiver. Detection of small amounts of AM that are a result of signal noise or other modulation formats is considered normal.

5.2.15 AM Output Low-pass Filter Selection

Both receiver types allow the application software to add a low-pass filter to the AM output. Three filter selections can be made along with a by-pass mode. Since the configuration PROM does not contain the cutoff frequencies for the filters, the cutoff frequencies are returned to the application software in *Status Register 6* and *Status Register 7*. Figure 5-12 below contains the registers associated with the AM output low-pass filter.

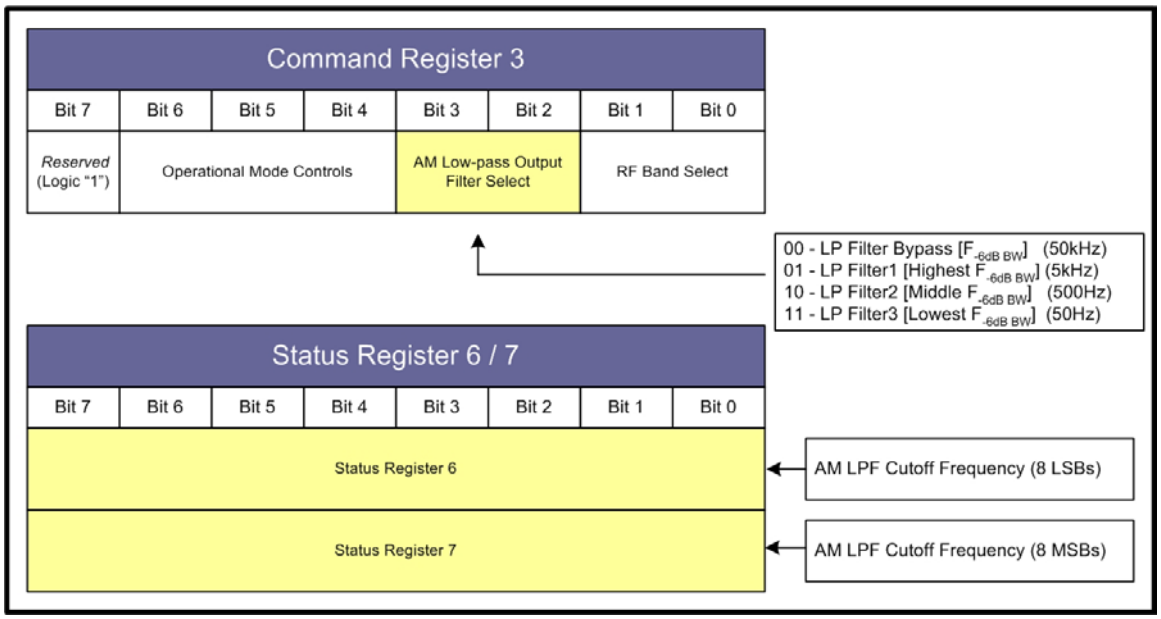


Figure 5-12 AM Low-pass Output Filter Command/Status

Selection of the AM Low-pass output filter should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)

2.) Enter the desired logic state in bits 3 and 2 of *Command Register 3*.
3.) Loop until the BUSY bit drops low. At this point, the cutoff frequency data will be available in *Status Register 6* and *Status Register 7*.

Information:
If it is desirable to have the application software display the available AM LPF cutoff frequencies, it is suggested that the application command each of the AM LPF selections at initialization to acquire the filter cutoff information.

5.2.16 AM Frequency Counter

The receiver design provides the application software with an AM frequency counter. Figure 5-13 below contains register definitions associated with this function.

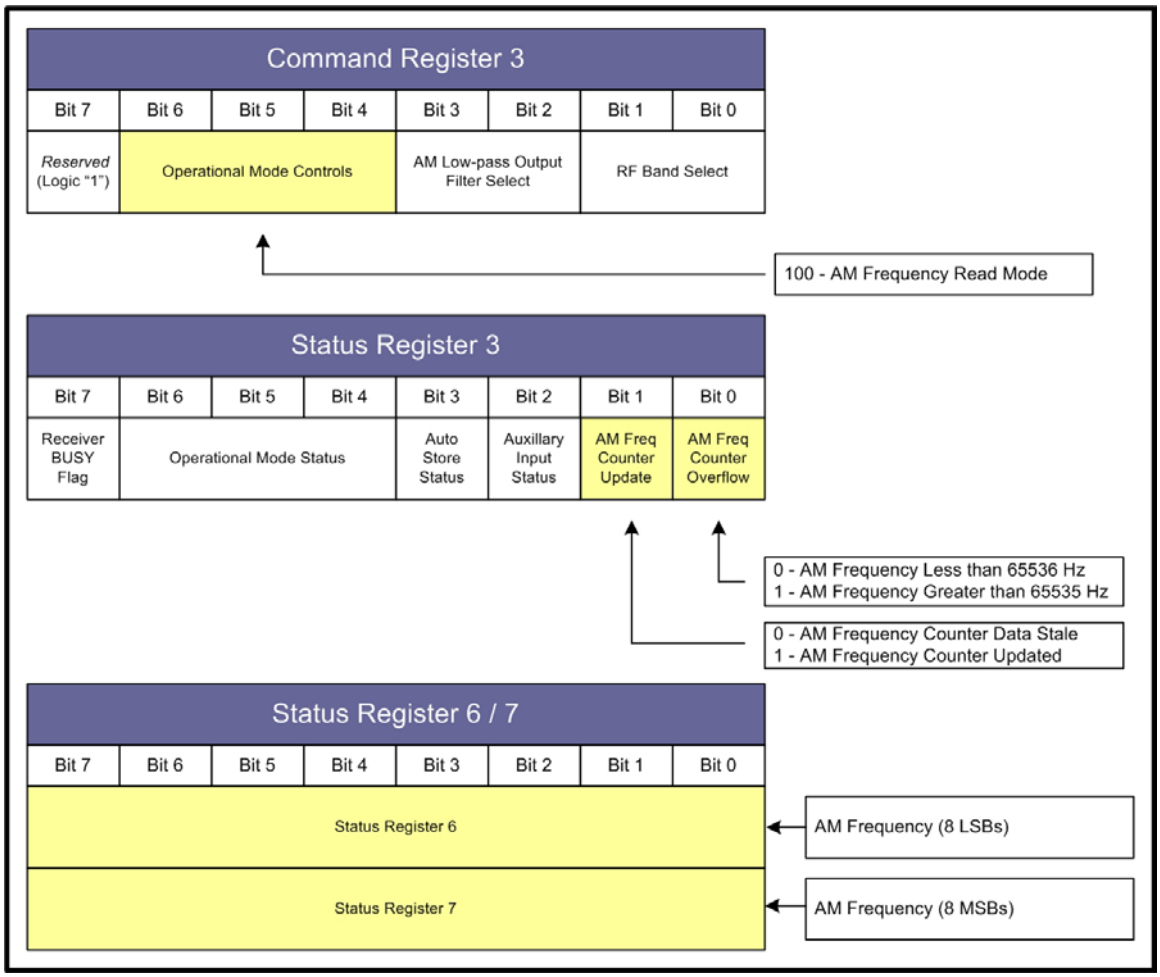


Figure 5-13 AM Frequency Counter Registers

Access to the AM Frequency Counter should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) The application software should monitor the AM Frequency Update flag and the AM Counter Overflow flag in host *Status Register 3*. If the AM Frequency Update flag is set, the AM Counter values are updated and available to be read by the application. If the AM Frequency Update flag is set, the application should take note of the state of the AM Counter Overflow flag. This flag indicates the whether the counter has overflowed indicating that the frequency values is greater than 65535 Hz. If this flag is set the host should add 65536 to the counter values read to determine the actual frequency.
3.) Once the AM Frequency Update flag is set, the AM Frequency Read Mode should be commanded by setting bits 6 through 4 of *Command Register 3* as follows: 100_b
4.) Once the mode command has been sent, the BUSY status flag will be set while the counter values are transferred to *Status Register 6* and *Status Register 7*.
5.) When the BUSY flag is low, the 8 LSBs of the counter value can be read from *Status Register 6* and the 8 MSBs of the counter value can be read from *Status Register 7*.

Caution:

The AM Frequency Counter is active during all phases of operation. Certain modulation formats and noise patterns may make the output values erroneous. It is suggested that the application provide a means to halt the display of this counter to reduce potentially confusing values.

Information:

Updates to the AM Counter are performed by on-board counters which have a 1Hz update rate. High-rate software monitoring of this value is unnecessary and wasteful.

5.2.17 AM Output Gain Controls

The receiver provides the application software gain control of the AM output signal. This control is provided via a "digital" potentiometer referred to in this documentation as a "Digipot". The AM output gain control Digipot contains 100 steps of gain adjustment. The controls may be individually stepped in either direction or be programmed to a specific setting via the application software interface. The device does not provide feedback of the actual setting so the application software must keep track of the control setting.

The AM output signal comes factory configured for a 2Vp-p output at an AM modulation depth of 50%. To increase the AM output voltage, the Digipot must be decremented in value. Conversely, to reduce the AM output voltage, increment the Digipot value. Figure 5-14 on page 47 contains the command registers associated with the AM Output Gain controls.

To individually step the AM Gain Digipot, follow this procedure:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Write a 0x02 to *Command Register 6*
3.) Set *Command Register 7* bits 1 and 0 to the achieve the desired step direction
4.) Set *Command Register 7* bit 7 to 1.
5.) When the BUSY flag goes low, the Digipot action is complete.

To program the AM Gain Digipot for a specified value, follow this procedure:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Write the desired value (0 to 99) to *Command Register 5*
3.) Write a 0x02 to *Command Register 6*
4.) Set *Command Register 7* bits 1 and 0 to: 10.
5.) Set *Command Register 7* bit 7 to 1.
6.) When the BUSY flag goes low, the Digipot action is complete.

Caution:
Completion times for individually stepped Digipot commands may be as long as 200 usecs. Full scale digipot commands may take as long as 40 msecs. These commands should be issued sparingly.

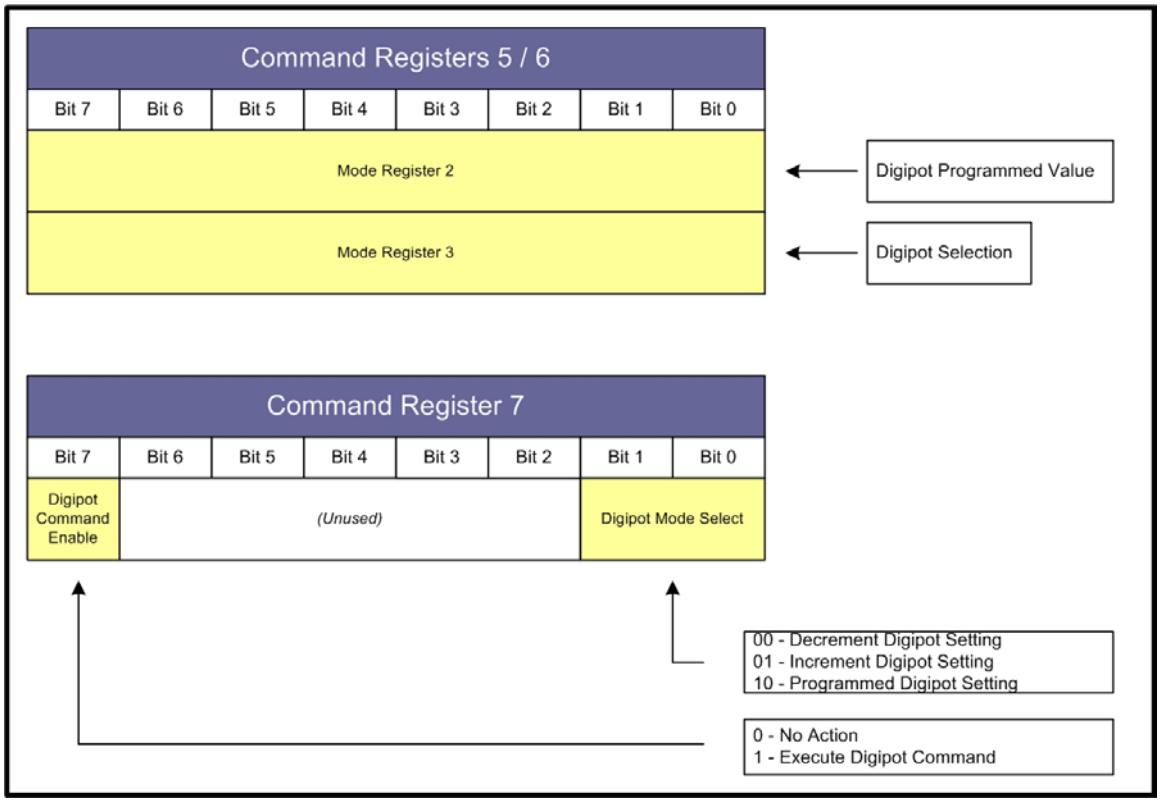


Figure 5-14 AM Output Gain Control

Information:

The Digipots are internally protected from accidental programming which extends beyond full-scale. If commanded to perform 125 incremental steps, the Digipot will stop at 99.

5.2.18 AGC Time Constant Selection

The first two bits of *Command Register 0* allow the application software to select an AGC Time Constant, which is applied to the RSSI Output found on the J5 connector. The time constants are related to the RSSI linearization processing that is being conducted via the DSP processor. As the time constant value is increased, the fundamental frequency of the DSP linearization process is decreased, thus reducing AM components in the RSSI output. Figure 5-15 below contains the AGC time constant selection.

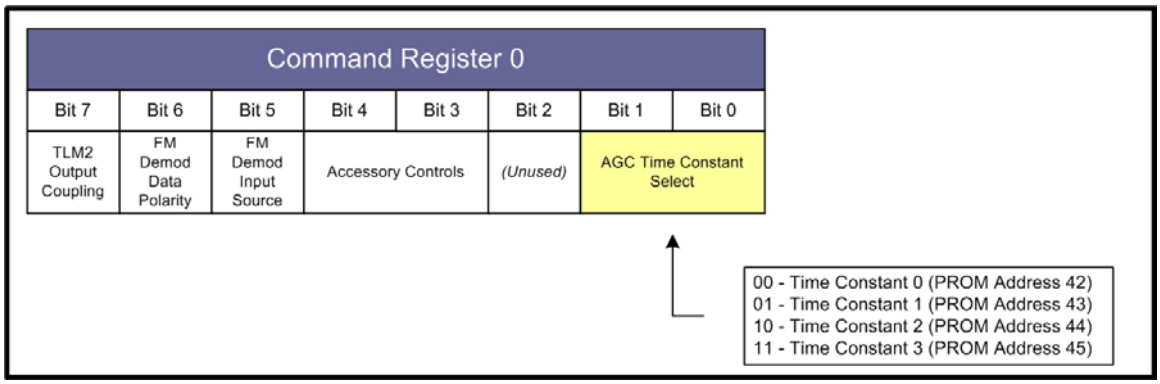


Figure 5-15 AGC Time Constant Selection

Selection of the AGC Time constant should follow the process below:

1.) Ensure that the BUSY bit is not set. (*Status Register 3*, bit 7)
2.) Enter the desired logic state in bits 0 and 1 of *Command Register 0*.

Information:

If it is desirable to have the application software display the available time constants, the software must multiply the values found in the configuration PROM by 100usecs.

5.2.19 Accessory Control Selection

Bits 3 and 4 of *Command Register 0* allow the application software to select Accessory Controls, found on the J3 connector. These controls provide TTL level output switching which may be used for customer specific applications. Figure 5-16 below contains the Accessory Control selection.

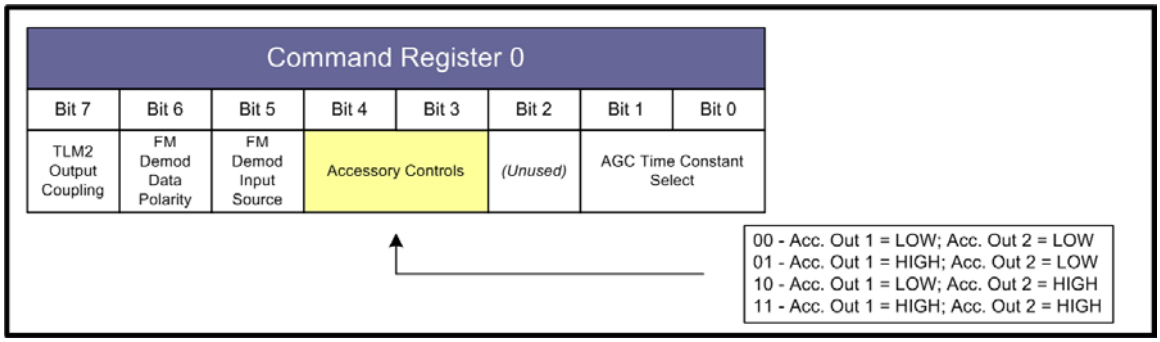


Figure 5-16 Accessory Output Selection

Selection of the Accessory Output Controls should follow the process below:

1.) Ensure that the BUSY bit is not set. (STAT3, bit 7)
2.) Enter the desired logic state in bits 3 and 4 of *Command Register 0*.

5.2.20 Auto-store Status

The receiver has the ability to store its presently programmed configuration and then automatically resume this state upon power-up. This function allows the receiver to be started without the necessity to initiate any control software, thus saving on start-up time. This function is initiated via switch SW1-2 (See Figure 3-3 on page 16). The parameters that are stored by this function are displayed in Table 5-3 below.

Auto-store Contents
AGC Time Constant Selection
FM Demodulator Input Selection
FM Demodulator Data Polarity Selection
TM2 Output Coupling Selection
IF Filter Bandwidth Selection
Video Filter Bandwidth Selection
RF Band Selection
Tuner Frequency
AM Output Gain Level
TLM Gain Adjustment for Video Filter 0
TLM Gain Adjustment for Video Filter 1
TLM Gain Adjustment for Video Filter 2
TLM Gain Adjustment for Video Filter 3
TLM Gain Adjustment for Video Filter 4
TLM Gain Adjustment for Video Filter 5
TLM Gain Adjustment for Video Filter 6
TLM Gain Adjustment for Video Filter 7
TLM Gain Adjustment for Video Filter 8
TLM Gain Adjustment for Video Filter 9
TLM Gain Adjustment for Video Filter 10
TLM Gain Adjustment for Video Filter 11
AM LP Filter Selection

Table 5-3 Auto-store Parameters

Some customers may have security concerns about data being stored by the receiver. To address this issue, a flag in *Status Register 3* indicates the state of this switch. Figure 5-17 below illustrates this bit.

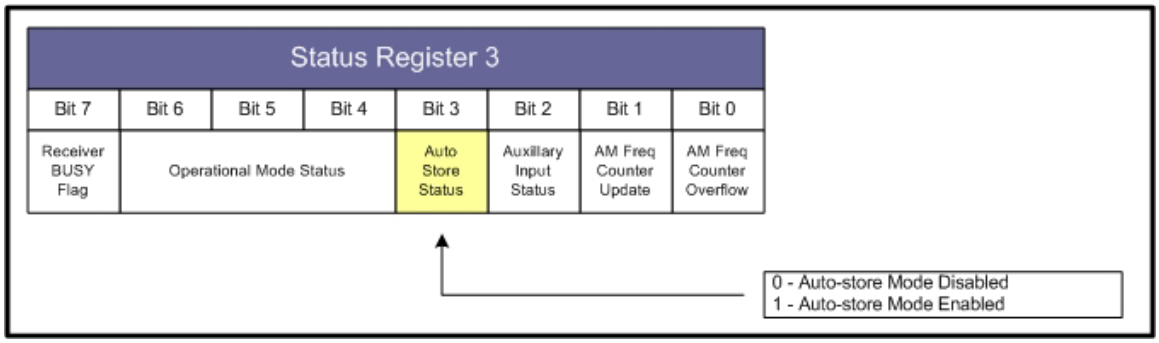


Figure 5-17 Auto-Store Function Status Flag

5.2.21 Auxiliary Input Status

The J5 connector provides an auxiliary TTL-level input to the receiver. This can be used by the application software to signal a change-of-state command or as a general-purpose status flag. The status of this input can be found in Status Register 3. Figure 5-18 below illustrates this input status.

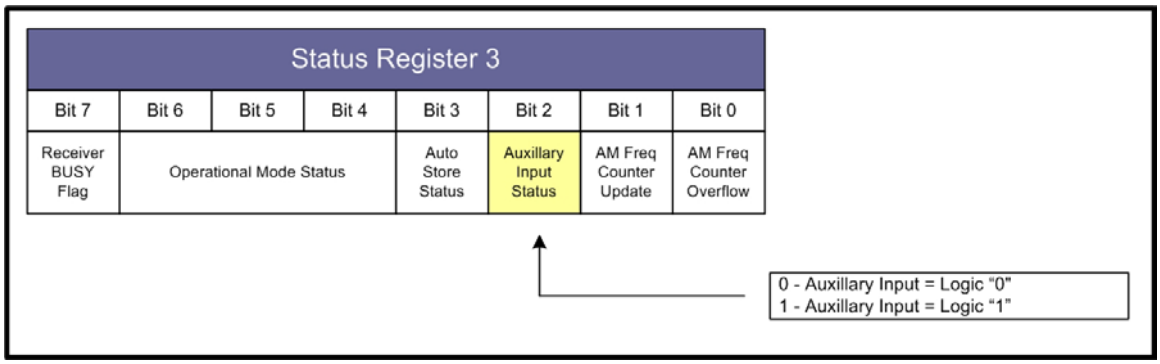


Figure 5-18 Auxiliary Input Status Flag