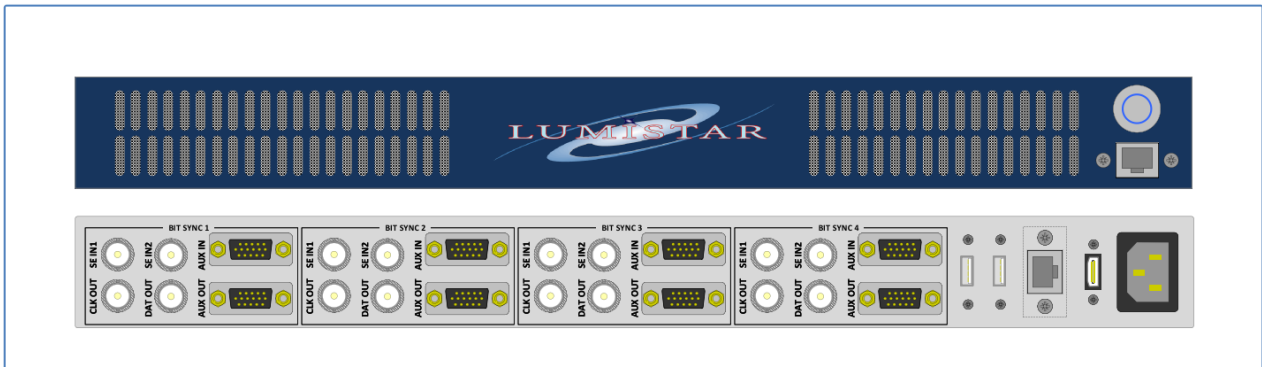


# LUMISTAR

## LS-45-QBS Four Channel Bit Synchronizer

### Data Sheet



LS-45-QBS Front and Rear Panel Elevations

### Description:

The Lumistar LS-45-QBS Four Channel Bit Synchronizer provides optimal reconstruction of a multiple serial PCM data streams that may have been corrupted by noise, phase jitter, amplitude modulation, or base line variations. The all-digital design assures a high performance, consistent product, with excellent reliability and long-term stability. The LS-45-QBS is available in single, dual, three and four channel versions and provides as an option for a post D diversity combiner that allows for best source combining of two input signals.

A unique Built-in-Test feature allows performance verification for the Bit Synchronizer to ensure the highest level of operation. *Auto-test BIT* is performed for a short duration on the application of power and tests more than 90% of the Bit Synchronizer components. This test verifies that power is properly applied, verifies that there are no internal bit errors, and performs other tests to ensure that the bit synchronizer is fully operational with status indication of results. After power on, *Command-test BIT* performs the same functions and can be initiated by the user at any time through the Lumistar software when used on Lumistar PC products. The user has the ability to generate internal pseudo-random patterns and calculate internal bit error rates with or without the injection of forced errors. Various status indicators are also available through the software. The Bit Synchronizer also contains a BER reader as well as frame sync pattern indicator.

### Key Features:

- **PCM Data Rates up to 45 Mbps for NRZ-L (22.5 Mbps for Bi-Phase/Miller)**
- **Performance to well within 1 dB of theoretical to 20 Mbps (2 dB to 45 Mbps)**
- **All Digital Design ensures high reliability and long-term performance**
- **One single ended TTL and one differential RS-422 input per channel**
- **Receiver Bit Error Rate Reader**
- **Low power consumption at less than 50 watts**
- **Built-in-Test with internal BER measurement and FSP reader**
- **Optional Viterbi decoding for rate  $\frac{1}{2} k=7$  (Others available consult factory)**
- **USB Interface**

## PCM Data Rate and Input Codes:

The LS-45-QBS Bit Synchronizers can operate over a range of 100 bits per second to their maximum data rate of 45 Mbps for all NRZ codes, or from 100 bits per second to 22.5 Mbps for the Bi-Phase and Miller codes.

NRZ codes :	NRZ-L, NRZ-M, NRZ-S, RZ codes
Split phase codes:	BI $\phi$ -L, BI $\phi$ -M, BI $\phi$ -S
Miller codes:	DM-M, DM-S, M <sup>2</sup> -M, M <sup>2</sup> -S
Randomized codes	RNRZ-L, RNRZ-M,
RNRZ-Randomization sequence:	2 <sup>11</sup> -1, 2 <sup>15</sup> -1, 2 <sup>17</sup> -1, 2 <sup>23</sup> -1

## Input and Signal Characteristics:

Inputs signals:	Single-ended or differential
No. of inputs	Eight each type
Input Impedance:	Shipped with 50 $\Omega$ , 75 $\Omega$ , 120 $\Omega$ , 1K $\Omega$ (Software Selectable)
Input Polarity:	Normal or Inverted
Input Signal Amplitude:	0.1 V pp to 10 V pp (nominal)
Maximum Voltage Input:	10V RMS for 50 $\Omega$ , 75 $\Omega$ and 120 $\Omega$ Inputs 25V RMS for 1K $\Omega$ Impedance
Maximum DC Offset:	$\pm$ 5V for 50 $\Omega$ , 75 $\Omega$ and 120 $\Omega$ Inputs $\pm$ 25 V for 1K $\Omega$ Impedance
Dynamic AC baseline:	Baseline variations up to 100% of the input signal at rates to 0.1% of the signal frequency for sinewave or sawtooth signals (100 Hz max)
De-randomizer	11, 15, 17 and 23 bit both forward and reverse

## Phase-Locked Loop Performance:

Loop-Bandwidth:	Programmable from 0.001% to 5% depending on the Bit Rate
Acquisition Range:	0.04% to 8% depending on the Loop-Bandwidth selected
Tracking Range:	0.1% to 20% depending on the Loop-Bandwidth selected

## Bit Error Rate Performance:

The LS-45 Bit Synchronizer performance relative to theoretical is indicated below when the applied signal has a S/N ratio within 1dB of the specified synchronization threshold with a Gaussian white noise bandwidth up to three times the bit rate, and has no jitter or base line variations on the input signal.

<u>Codes:</u>	<u>Bit Rate:</u>	<u>Degradation from Theory:</u>
NRZ	<20 Mbps	< 1 dB max (0.5 dB typical)
NRZ	20 to 30 Mbps	< 1.5 dB max (1 dB typical)
BI $\phi$ , RZ	<10 Mbps	< 1 dB max (0.5 dB typical)
BI $\phi$ , RZ	10 to 15 Mbps	< 1.5 dB max (1 dB typical)
DM, M <sup>2</sup>	up to 15 Mbps	< 2 dB max (1 dB typical)

## Capture Threshold:

The Capture Threshold when the applied signal has a S/N ratio within 1 dB of the specified synchronization threshold, has a Gaussian white noise up to three times the bit rate, and has no jitter or base line variations on the input signal is defined below:

<u>Codes:</u>	<u>Capture Threshold:</u>
NRZ	-1 dB (-3 dB typical)
BI $\phi$	+1 dB (+0 dB typical)

The capture range of the bit sync is up to  $\pm$  5% of the bit rate

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## LS-45-QBS Four Channel Bit Synchronizer

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#### Synchronization Hold:

The LS-45 Bit Synchronizer is capable of maintaining synchronization during periods of signal loss or during continuous periods of 1s or 0s lasting up to 245 bits in every 1024 bits, for NRZ coded signals up to 5 Mbps or BI $\phi$  coded signals up to 2.5 Mbps, providing:

- S/N ratio is greater than 12 dB
- PLL bandwidth is equal to 0.1%
- 50% Transition Density when the signal is present
- Input signal has no jitter or base line variations
- Signal has a constant amplitude

#### Acquisition Time:

The mean acquisition time is a function of the Loop Bandwidth and will be less than 100 bits with a Loop Bandwidth of 1% and less than 150 bits with a Loop Bandwidth of 0.1% for NRZ signals up to 5 Mbps or BI $\phi$  signals up to 2.5 Mbps, providing:

- Gaussian white noise in a band up to three times the bit rate
- Transition Density is greater than 2% of the bit rate
- Signal has no jitter or baseline variations on the input signal

#### Viterbi Decoding (Optional):

Rates 1/2, ( Consult Factory 2/3, 3/4, 5/6, 7/8)  
Constraint Length k=7  
Puncture Matrix Per NASA Standards

#### Output Signals:

Data	TTL and RS-422 Driven
Clock	TTL and RS-422 Driven
	0°, 90°, 180°, 270° phase adjustments
Tape Outputs	1 V pp into 50 $\Omega$ (code programmable) TTL and RS-422
Lock Status	In Status Register
Es/No >5dB Status	In Status Register
Input Signal Level Status	In Status Register
Built-in-test	In Status Register

#### Environmental:

Temperature (Operating)	0 to 50 °C
Temperature (Non-Op)	-25 to +70 °C
Humidity (Operating)	10% to 90% Non-Condensing

#### Physical:

1U chassis x 12" depth, 19" wide  
75 Watt power consumption, 110-220 VAC, 50-60 Hz

**Ordering Information:** Single Channel = LS-45-QBS-1 ; Dual Channel = LS-45-QBS-2  
Three Channel = LS-45-QBS-3 ; Quad Channel = LS-45-QBS-4

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*Specifications are subject to change. Please verify the latest specifications at time of order.*

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