



LS-26 Series

Quick-Start Guide

Airborne Receiver with Bit Synchronizer Version 6

With the following capabilities

Receiver

Bit Synchronizer

Link Analyzer

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1. Software Installation and Hardware Connection

1.1 Software Installation

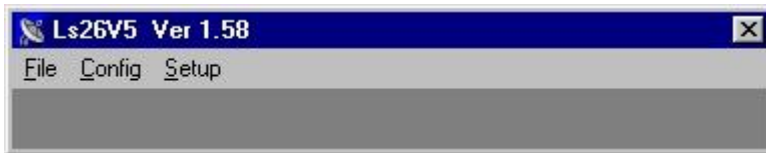
Install the LS-26V5 software on a PC with an RS-232 port. The installation will create an ICON on the desktop which can be used to start the application as shown below:



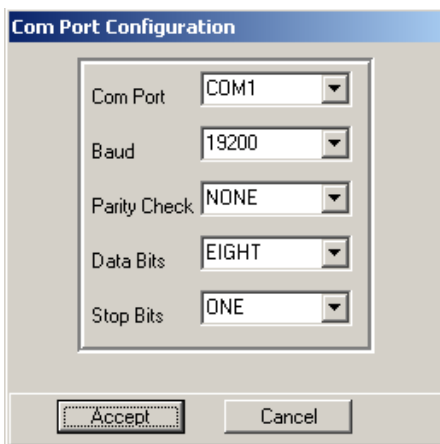
1.2 Hardware Connection

Connect the LS-26 Airborne Receiver / Bit Sync to the PC through an RS-232 data link using the programming cable provided.

Click on the ICON on your desktop and the following menu will appear.



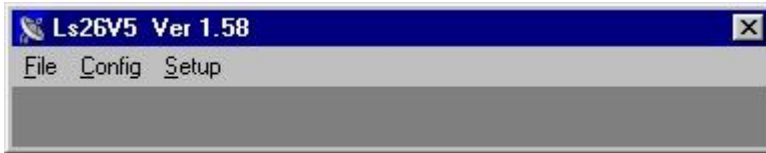
Click on **C**onfig, then **C**ommunications, and the default communications menu will appear for communicating from the computer to the LS-26 through the RS-232 port. The default communications menu is shown below:



These values cannot be changed with the LS-25-V5 Setup Program. Click on Accept to use the default communications settings. If other values are desired, please consult Lumistar.

2.1 Receiver Setup and Display:

Click on Setup from the following menu:



The following window allows setup of Receiver, Bit Synchronizer, and the Link Analysis sections of the LS-26. Select the Rcvr Setup Tab.

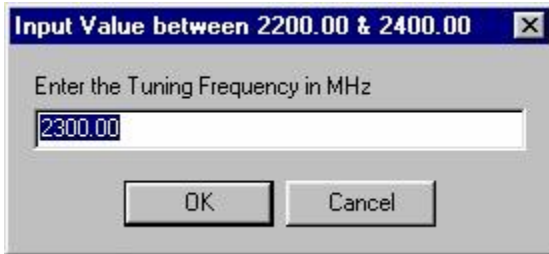


Right click over any of the values and you will get the following window:

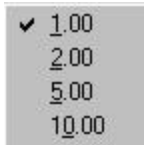


The software will read the frequency range available in your particular the LS-26. Right click on Freqs Avail and the frequency range will be shown.

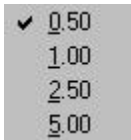
Right click on “Tuner Frequency” and you will be able to select the appropriate frequency of operation:



Right click on IF Bandwidth to select the desired IF Bandwidth.



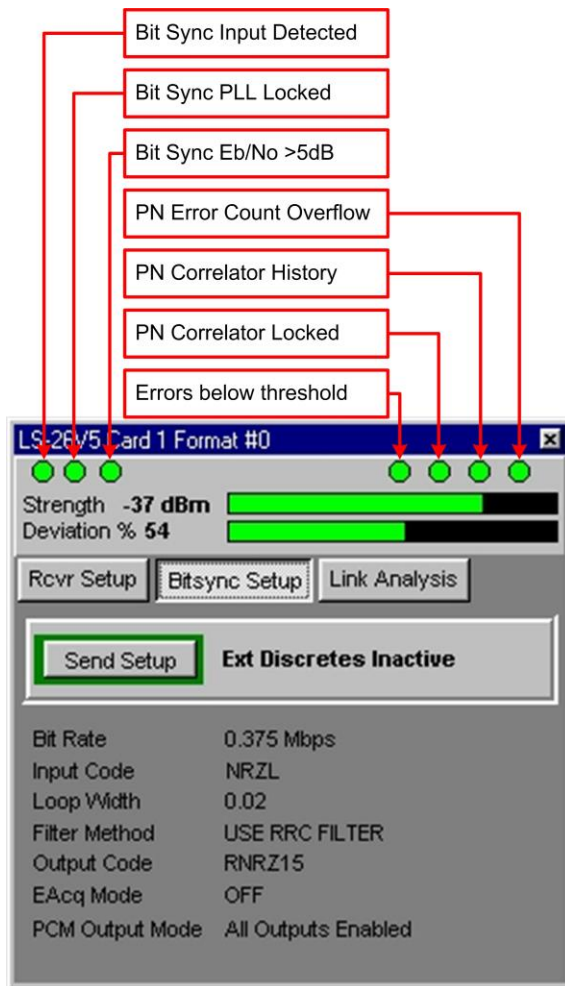
Right click on Video Filter Bandwidth and you can select the appropriate Video Filter.



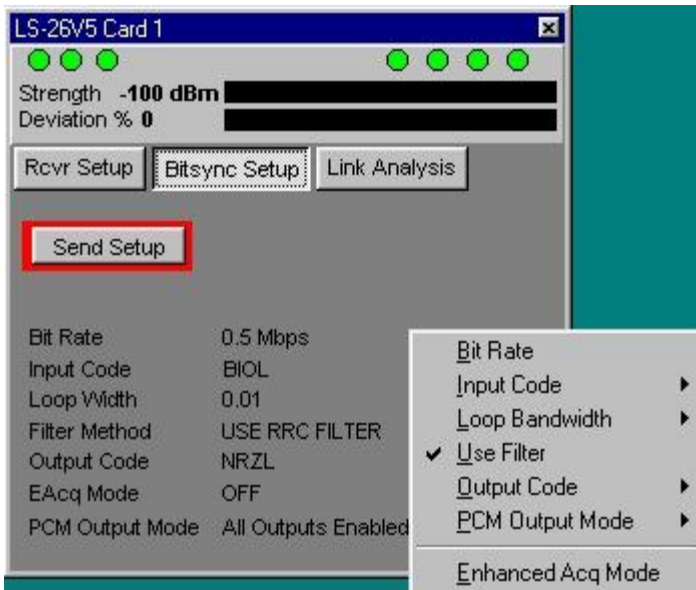
The filter value will default to 50% of the IF Bandwidth unless you select another filter.

2.2 Bit Synchronizer Setup

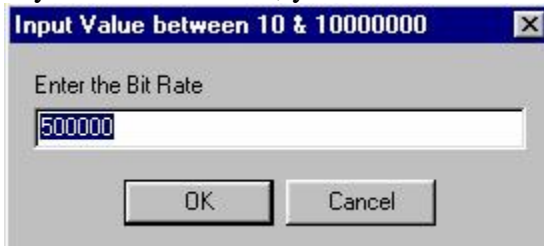
The bit sync tab includes a number of indicators that provide information concerning the state of the bit sync and the receive BERT PN correlator. The following diagram indicates their functions:



When you do a right click over the bit sync parameters, you will see the following menu:



If you select Bit Rate, you will see the following window. Enter the bit rate desired



If you select Input Code, you will see the following. Select the desired Input Code.

NRZL
NRZM
NRZS
BIOL
BIOM
BIOS
DMM
DMS
MDMM
MDMS
INV_NRZL
INV_BIOL
RZ
INV_RZ
RNRZ11
RNRZ15
RNRZ17
RNRZ23
INV_NRZM
INV_NRZS
INV_BIOM
INV_BIOS
INV_DMM
INV_DMS
INV_MDMM
INV_MDMS
INV_RNRZ11
INV_RNRZ15
INV_RNRZ17
INV_RNRZ23

If you select Loop Bandwidth, you will see the following. Select the desired Loop Bandwidth.

2.0
1.0
0.5
0.2
0.1
0.05
0.02

You can select USE RRC FILTER (Raised Root Cosine Filter) for tape playback applications which have rounded edges on the waveform. Normal operation should have the Filter OFF.

If you select PCM Output Code, you will see the following. Select the desired PCM Tape Output Code.

- NRZL
- NRZM
- NRZS
- BIOL
- BIOM
- BIOS
- DMM
- DMS
- MDMM
- MDMS
- INV_NRZL
- INV_BIOL
- RZ
- INV_RZ
- RNRZ11
- RNRZ15
- RNRZ17
- RNRZ23

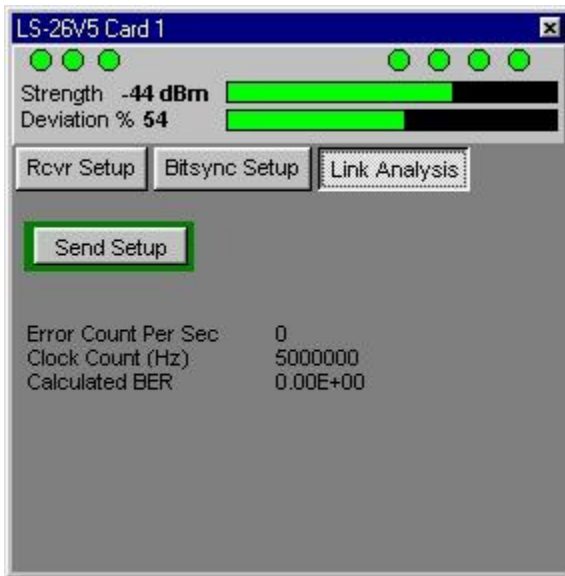
If you select PCM Output Mode, you can enable or disable the outputs as shown below:

- All PCM Outputs Disabled @ PLL Unlock
- All PCM Outputs Disabled @ Es/No < 5 dB
- PCM Tape Out Disabled @ PLL Unlock
- PCM Tape Out Disabled @ Es/No < 5 dB
- All PCM Outputs Enabled

Enhance Acquisition Mode (On/Off) can be selected. Normal operation is to use the Enhanced Acquisition Mode Off. This allows maximum frequency sweep for bit sync search, maximum course AGC, and maximum Baseline control. Enhanced Acquisition Mode is used to minimize acquisition time by the tightening the loops.

2.3 Link Analyzer Setup and Display

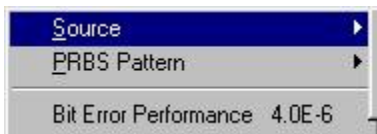
The LS-25SB contains the ability to measure bit error performance using the internal Link Analyzer. The Link Analyzer allows the use of either internal or external Psuedo Random Bit Stream (commonly called PRN generator) and an internal PRN reader to measure bit error rates. The display below shows error free operation with a 5 Mbps data rate.



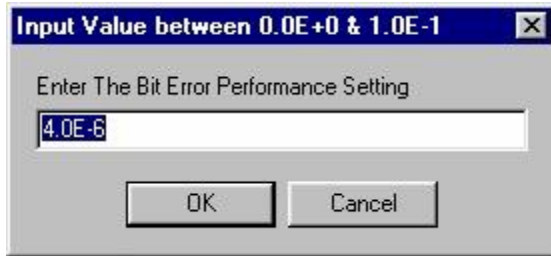
To setup the Link Analyzer right click over the values and you will see the following.



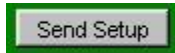
The PRBS Source can be selected to be "Internal" or "External" by right clicking on PRBS Source. External could be from a laboratory type Bit Error Test Set or the Lumistar LS-50-P Multi-Function Decom Simulator operating in BERT mode. Internal is the PRBS in the LS-26. PRBS Pattern can be selected for 11 or 15 by right clicking on PRBS Pattern. Bit Error Performance is displayed in the window and also sets a flag if the value is equal to or greater than the value set.



To set up the Bit Error flag, right click on Bit Error Performance and the following will be displayed:



When the Receiver, Bit Synchronizer, and Link Analyzer are set up, you can click on

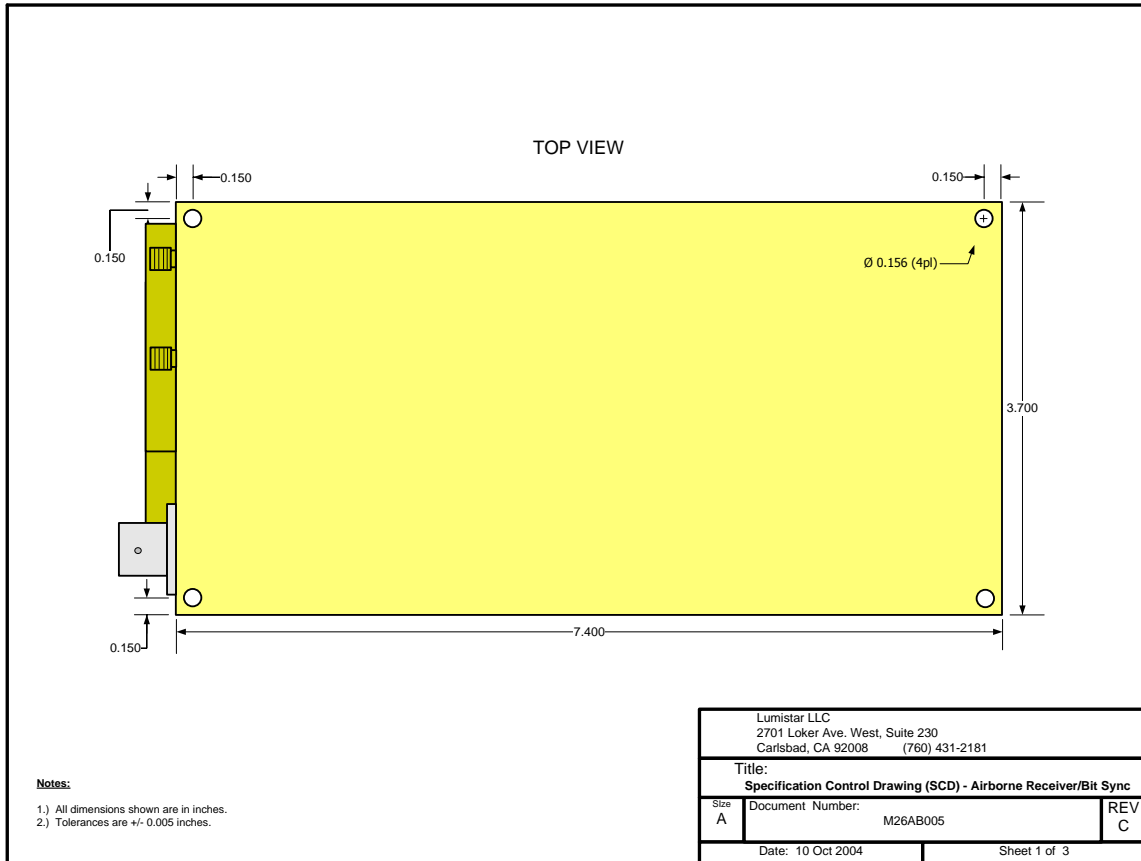


You will see the following.

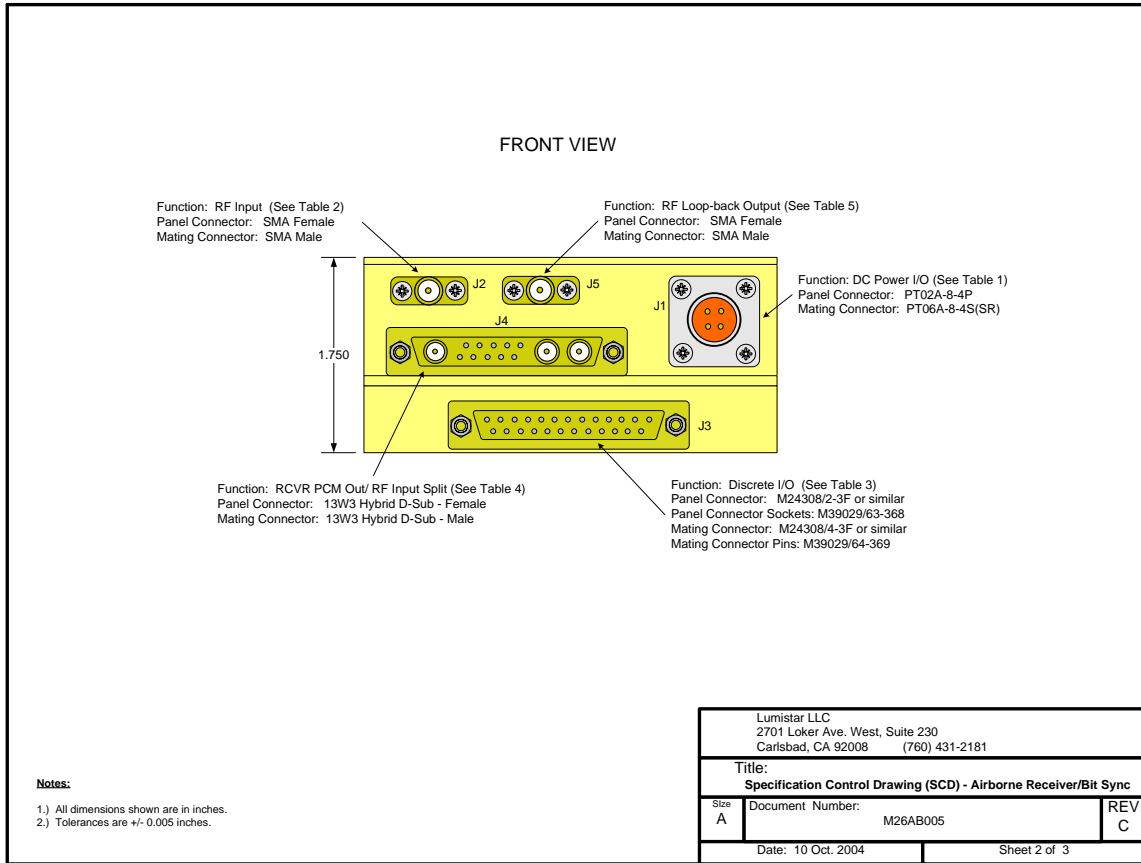


3. Drawings

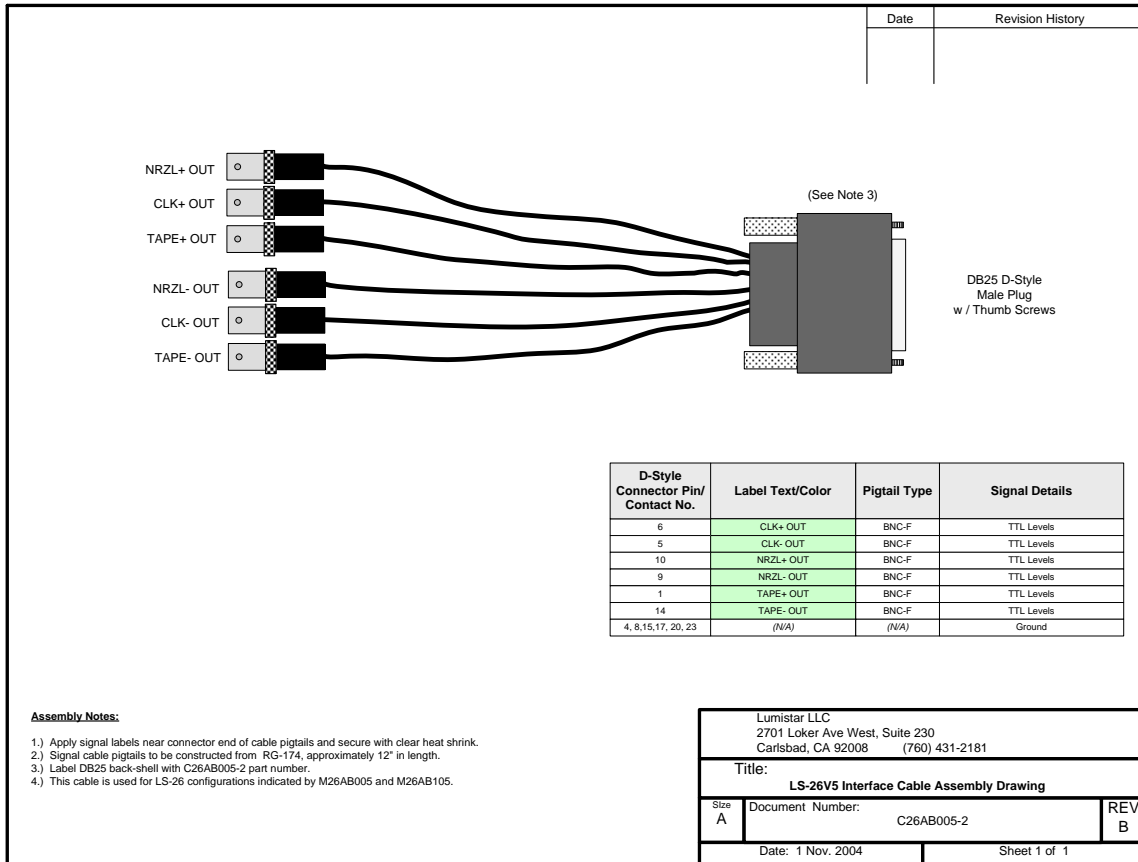
3.1 Outline Drawing - Top View



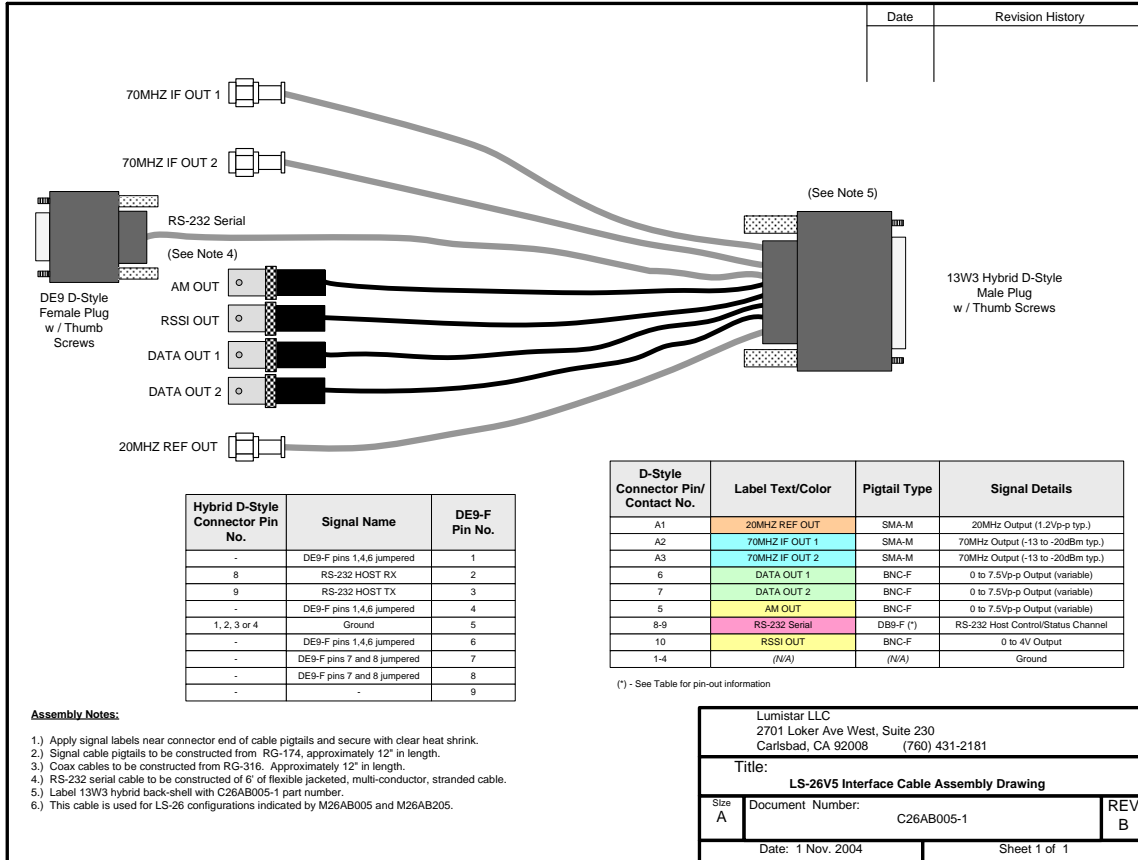
3.2 Outline Drawing - Connector Face



3.3 Cable Assembly - Bit Synchronizer Outputs



3.4 Cable Assembly - Programming



| Table 1. J1 Pin Definitions | |
|-----------------------------|---------------------|
| Pin A | +28VDC Power Input |
| Pin B | +12VDC Power Output |
| Pin C | +28VDC Return |
| Pin D | +12VDC Ground |

| Table 2. J2 Definition |
|------------------------|
| RF Signal Input |

| Table 3. J3 Pin Definitions | |
|-----------------------------|-------------------------|
| Pin 1 | PCM Tape Out (+) |
| Pin 2 | BS SIGQ Output |
| Pin 3 | BS THRES Output |
| Pin 4 | Ground |
| Pin 5 | CLK Out 1 (-) |
| Pin 6 | CLK Out 1 (+) |
| Pin 7 | Signal/Link Quality Out |
| Pin 8 | Ground |
| Pin 9 | NRZL Data Out 1 (-) |
| Pin 10 | NRZL Data Out 1 (+) |
| Pin 11 | (Unused) |
| Pin 12 | (Unused) |
| Pin 13 | (Unused) |
| Pin 14 | PCM Tape Out (-) |
| Pin 15 | Ground |
| Pin 16 | BS PLL Output |
| Pin 17 | Ground |
| Pin 18 | CLK Out 2 (-) |
| Pin 19 | CLK Out 2 (+) |
| Pin 20 | Ground |
| Pin 21 | NRZL Data Out 2 (-) |
| Pin 22 | NRZL Data Out 2 (+) |
| Pin 23 | Ground |
| Pin 24 | +28VDC Supply Reference |
| Pin 25 | (Unused) |

| Table 4. J4 Pin Definitions | |
|-----------------------------|------------------------|
| Pin 1 | Ground |
| Pin 2 | Ground |
| Pin 3 | Ground |
| Pin 4 | Ground |
| Pin 5 | AM Out |
| Pin 6 | TLM1 Out |
| Pin 7 | TLM2 Out |
| Pin 8 | RS-232 Host RX |
| Pin 9 | RS-232 Host TX |
| Pin 10 | RSSI Out |
| A1 | 20MHz Reference In/Out |
| A2 | 70MHz IF Out 1 |
| A3 | 70MHz IF Out 2 |

| Table 5. J5 Definition |
|---------------------------|
| RF Input Signal Loop-back |

| Receiver Specifications/Notes: | |
|---|--|
| 1.) RF Input: | 2200.5-2399.5 MHz |
| 2.) RF Tuning Step: | 500 kHz (typ.) 50 kHz steps (min.) |
| 3.) Maximum RF Input Signal without damage: | +14 dBm |
| 4.) Maximum RF Input before compression: | -2 dBm |
| 5.) RF Input Dynamic Range: | 80dB |
| 6.) Receiver AGC range: | -10 to -90dBm |
| 7.) VSWR: | 2:1 Max; 1.5:1 typical |
| 8.) Frequency Accuracy: | 0.002 ppm |
| 9.) Noise Figure: | 10dB max.; 7.5dB typical |
| 10.) RF Input Impedance: | 50 ohms |
| 11.) IF Frequency: | 70MHz |
| 12.) Receiver Data Outputs: | 4Vp-p (unloaded) |
| 13.) FM Demodulator bandwidth: | 12MHz (max.) [20Mbps NRZL data] |
| 14.) DC Input Power: | 24-32VDC@ 500mA (typ.) 700mA (max.) |
| 15.) DC Output Power: | 12VDC@150mA (max.) |
| 16.) Receiver Discrete Outputs: | Open Collector; 35VDC Breakdown voltage; Ground when signal active |
| 17.) IF Filters (3dB BW) | (4 Bandwidths - Customer Specified) |
| 18.) Post Detect Filters (3dB BW) | (4 Bandwidths - Customer Specified) |

| Bit Synchronizer Specifications/Notes: | |
|--|---|
| 1.) Data Rates: | 50- 20Mbps NRZL; 50-10Mbps all other codes |
| 2.) PCM Input/Output Codes: | NRZ-L/M/S, BIO-L/M/S, DM-M/S, M2-M/S, Inv. BIO-L, Inv. NRZ-L, RZ, Inv. RZ, RNRZ-11/15 |
| 3.) PCM Tape Output: | +/- TTL levels |
| 4.) PCM Clk/Data Outputs: | +/- TTL levels |
| 5.) THRES/PLL/SIGQ/Setup Complete Outputs: | Open Collector; 35VDC Breakdown voltage; Ground when signal active |

| Control Interface Notes: | |
|---|--|
| 1.) All bit synchronizer and receiver control and status commands via an RS-232 serial link @19.2Kbps. | |
| 2.) All settings are retained in internal EEPROM. | |
| 3.) Link analysis functions allow an external PRN-15 source to be utilized to test end-to-end link functionality. | |
| 4.) Design allows airborne receiver to be sold with or without Bit Sync option. | |
| 5.) Signal Quality TTL output will be active during normal operations when Es/No levels are >5dB. | |
| 6.) During external link testing modes, this TTL will be active when detected link Bit Error Rates are < 1x10E-6. | |

| | | |
|--|------------------------------|--------------|
| Lumistar LLC 2701 Loker Ave. West, Suite 230 Carlsbad, CA 92008 (760) 431-2181 | | |
| Title: Specification Control Drawing (SCD) - Airborne Receiver/Bit Sync | | |
| Size A | Document Number: M26AB005 | REV C |
| Date: 10 Oct. 2004 | | Sheet 3 of 3 |