LS-22-SE

Hardware User's Manual

Spectral & Oscilloscope Display PCI Card

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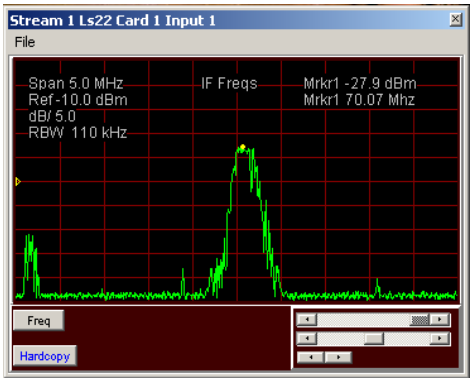
1 INTRODUCTION

1.1 General

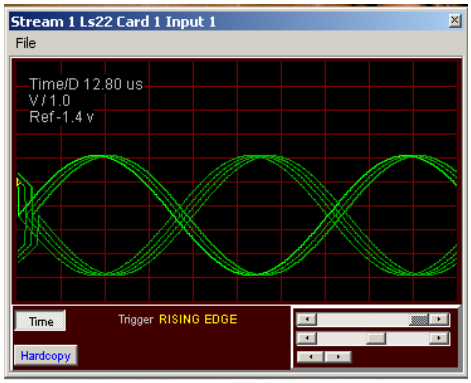
This document is the Hardware User's Manual for the Lumistar **LS-22-SE** Spectral & Oscilloscope Display PCI Card. The intent of this document is to provide physical, functional, and operational information for the end user including hardware configuration, interconnection and software interfaces for the device.

Table 1-1 on page 7 contains a detailed model number construction for the LS-22-SE series. This document applies to all model combinations indicated in the table. Optionally, the Lumistar **LS-40-DB10** or **LS-40-DB20** Bit Sync Daughterboard may also be installed on the LS-22-SE Series. Consult the factory for a copy of the LS-40 documentation. Hardware related setup and interface information can be found in the LS-40 Series User's Manual (Doc. No. U4000201).

The Lumistar LS-22-SE series Spectral & Oscilloscope Display PCI Card is designed to allow spectral and eye pattern displays when used in concert with receivers and diversity combiners.



Spectral Display



Time Domain Display (eye pattern)

There are three variants in the LS-22-SE series, with single, dual, and triple channel versions available. The LS-22-SE is a single channel instrument that supports the display of spectral and oscilloscope information using the Lumistar Data Processing System (LDPS) software (shown above). The single channel LS-22-SE variant only supports the selection of one type of display at a time (spectrum or time domain). The simultaneous display of both spectral and eye pattern is achievable with the dual channel LS-22-2SE. The simultaneous display of three input channels (in any combination) is supported by the LS-22-3SE.
LS-22-SE series key features:

- A spectral display with up to 20 MHz Bandwidth - accepts 70 MHz IF inputs from the LS-25P-2 Receiver or LS-23-P Pre-Detection Combiner and displays up to 3 spectrums depending on the model selected.
- An Oscilloscope with a sampling rate of 40 MSPS- accepts and selects one of 3 input channels of analog information such as baseband data, bit synchronized data, or AM waveform displays.
- Accepts the LS-40-DB Bit Synchronizer Daughterboard to output data & clock.
- A PCI board with 7.525 inch length.
- Uses the LDPS Software allowing setup, control, and display of LS-25 Series of Receivers and LS-23 series of Diversity Combiners.

Table 1-2 on page 9 provides specifications for electrical, mechanical, and operational characteristics of the LS-22-SE series product line. A block diagram of the product design is shown in Figure 1-1 on page 10.

Table 1-1 Applicable Models

Without Bit Synchronizer	LS-22-SE (Single Display)
	LS-22-2SE (Dual Display)
	LS-22-3SE (Triple Display)
With Bit Synchronizer	LS-22-SEB (Single Display)
	LS-22-2SEB (Dual Display)
	LS-22-3SEB (Triple Display)

1.2 Manual Format And Conventions

This manual contains the following sections:

- Chapter 1 provides a brief product overview and technical specifications
- Chapter 2 provides the theory of operation
- Chapter 3 provides installation and configuration instructions
- Chapter 4 provides info on the LS-22-SE LDPS software
- Chapter 5 provides programming information

Throughout this document, several document flags will be utilized to emphasis warnings or other important data. These flags come in three different formats: Warnings, Cautions, and Information. Examples of these flags appear below.

Warning:

(Details of critical information which prevents loss of functionality)

Caution:

Details of operational or functional cautionary advisories

Information:

(Details of emphasised operational information)

Table 1-2 Specifications for the LS-22-SE Series		
Mechanical		
	Envelope Dimensions	7.5"(L) x 3.9"(W) x 0.74"(H)
	Form Factor	PCI board – 7.5 inch long
	Weight	~ 6 oz.
	Daughterboard	Accepts LS-40-DB Bit Synchronizer
Electrical		
	Individual power requirements	+5 V = 680ma
	Current Required (typ)	+12 V = 25ma
		-12 V = 10ma
	Total Power	< 3.8 Watts
Performance		
Spectral Display Inputs:	Display Bandwidth	Up to 20 MHz
	Number of Channels	Up to 3 depending on the model chosen
	Input Frequency	70 MHz IF
	Input Signal Level	-20 dBm Nominal
Oscilloscope Display Inputs:	Oscilloscope Bandwidth	40 MHz sampling rate Approx. 8 MHz
	Number of Channels	Up to 3 depending on the model chosen
	Baseband PCM Inputs	Baseband PCM inputs can be simultaneously applied to the scope and optional bit synchronizer.
	Other Analog Inputs	Oscope can also monitor: Bit Synchronizer output, AM Output from LS-25, AGC Output from LS-25, etc…
	Input Signal Level	4 Volts p-p for full-scale
Bit Synchronizer Outputs:	NRZ-L Data and Clock	TTL Level
	Tape Output	PCM Code selectable bi-polar output for Instrumentation tape recorder
	Test Output	Pseudo-random test pattern can be enabled from the bit synchronizer with 2^{15}-1 PRN sequence. This output is bi-polar.
Other Inputs & Outputs:	Status	A TTL-compatible status line is provided
	Aux Status Triggers (up to 3)	Used for external trigger input for the oscilloscope display
	Auxiliary Bit Sync Input	Used when bit sync is not associated with scope
Connectors		
	IF Input Connections	Three (3) SMA Type
	Other I/O	D-Series Connector with 26 female contacts.
	Breakout Cable	Cable assembly to BNC included
Environmental		
	Operating Temperature	0° to $+50^o$ C
	Non-Operating Temp	-25° to $+70^o$ C
	Operating Humidity	0 to 90% (Non-condensing)
	Non-Operating Humidity	Protect from moisture and contamination

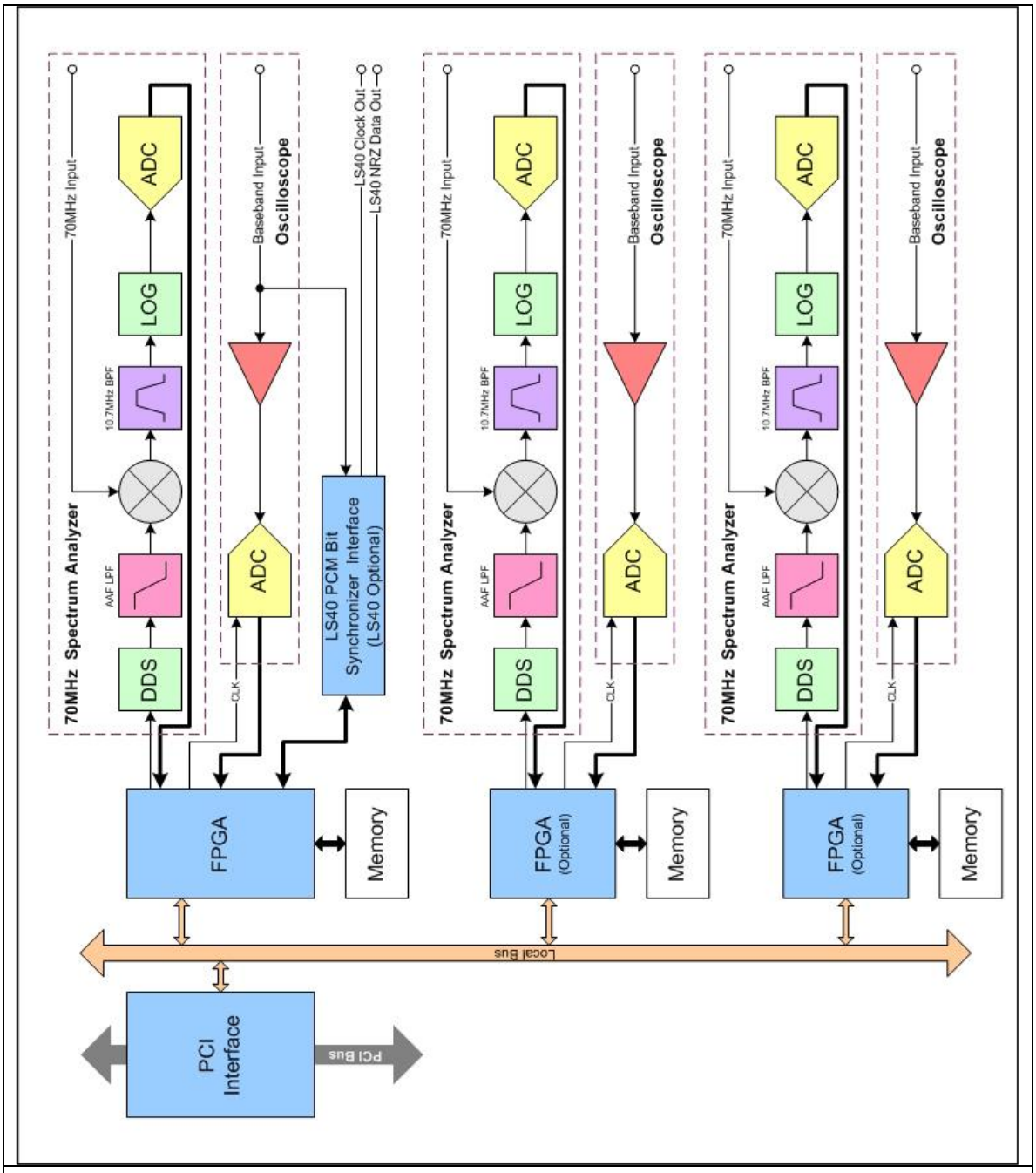


Figure 1-1 Block Diagram of the LS-22-SE Series Display Card

2 THEORY OF OPERATION

This section of the document discusses the theory of operation of the LS-22-SE Spectral & Oscilloscope Display PCI Card from a functional perspective. The discussion will focus on the main functions the board performs and will include:

- Spectrum Analyzer
- Oscilloscope
- FPGA
- PCI Interface
- Input Channels

The functional block diagram for the LS-22-SE is shown in Figure 1-1 on page 10.

2.1 Input Channels

The LS-22-SE is populated with either, one, two, or three "channels." Each channel implements either a spectral display centered at 70MHz or a digital oscilloscope. For each channel, a Xilinx FPGA controls these functions and interfaces them to the local address and data bus of a PLX Technologies PCI9080 PCI interface chip. The 9080 is the primary interface between the LS-22-SE and the computer system it is installed in. The first channel is always populated and performs some additional functions not found in the other two channels (LS-40 interface for example).

2.2 Spectrum Analyzer Functionality

To obtain a spectral plot, a Numerically Controlled Oscillator (NCO) is initially programmed to run at a frequency that is equal to 59.3 MHz, minus one half of the sweep range. The NCO output has many extraneous frequencies that are knocked down by a passive LC filter. The filtered signal drives the IF input of a mixer. The other input of the mixer is a 70MHz (nominal) IF output from a receiver or combiner and is brought in and amplified prior to mixing. The mixer output is buffered and then passed through two, 10.7 MHz ceramic bandpass filters. The 10.7 MHz result is monitored by a LOGAmp. The leveled output of the LOGAmp is not used but its VLOG output is conditioned and sampled by a LTC1199, 10-Bit, 500ksps A/D converter.

During the acquisition of the spectral samples, the controlling application issues commands that initializes the NCO to begin running at the bottom frequency of the sweep range. The ceramic bandpass filters create a "window" about 150 kHz wide at this point. The A/D converter samples the LOGAmp output, and the NCO is then stepped up 1/128 of the sweep range (moving the window). The A/D samples again, and so on until 128 consecutive samples have been taken. As the samples are taken the results are stored away in RAM. A status register sets a flag when the last sample has been taken. The controlling application can then issue an address reset command and reads the RAM contents out by sequential two-byte reads of the I/O space. It should be noted that the spectrum analyzer data is logarithmic and unipolar and is represented in offset-binary format.

2.3 Oscilloscope Functionality

The baseband input signal(s) of the LS-22-SE are first buffered and level-shifted to establish them within the range of an AD9050, 10-Bit, 40-MSPS high-speed flash A/D. The A/D clock is provided by the FPGA. The A/D samples are latched into a register and connected directly to the RAM. To initiate a sample, the controlling application issues an I/O command to arm the scope. The scope control logic in the FPGA is set to trigger on either a zero-crossing at the input, or on an externally-supplied trigger pulse. The scope logic can also free-run and trigger immediately. When the scope triggers, 256, 512, or 1024 samples are taken at the A/D clock rate. At slower sample rates, the A/D is "over-clocked" and the output decimated (most of the data thrown away). As with the spectrum analyzer, a done-status indicates the sampling is complete and the data can be read out sequentially.

2.4 FPGA Functionality

On the LS-22-SE, most of the logic associated with a "channel" is implemented in a Xilinx FPGA. The Xilinx part is a programmable "soft" device, and is initialized from a serial EEPROM. At system reset time, this EEPROM is sequentially read from and the Xilinx part is configured. If additional channels are populated, each of them will have their own FPGA but will be programmed in parallel with data from the EEPROM.

The FPGA provides data and timing signals to the spectrum analyzer and scope functions for each channel. In the case of the channel 0 FPGA, it also controls the timing of the data bus and address bus connected to the PCI9080 PCI interface chip.

A second EEPROM is associated with channel 0. This EEPROM is organized into 16-bit words and in this application is pre-initialized to provide the following: First, a null-bound ASCII string up to 15 bytes long is pre-stored in this EEPROM (specifically, "LS22SE") and is read out immediately after the FPGA is initialized. This string is stored in a small RAM inside the FPGA and can be sequentially read through I/O port 0xn0. For channel 0, this can be used to confirm the board is indeed an LS-22-SE. For the other channels, it can be used to determine their presence. Second, the spectrum analyzer has four sweep widths defined. The sweep function is implemented by an NCO. The starting NCO frequency, and the "increment" for each sweep are stored in the EEPROM as 32-bit constants. This enables the FPGA to operate the analyzer sweep function without processor mothering.

Third, the channel 0 FPGA uniquely drives the board ID function. This is implemented by four chip LEDs mounted along the top edge of the board. These indicators have two purposes. As the LS-22-SE has no real power-up diagnostics, the LED indicators are physically connected in such way that during system reset, and until the FPGA(s) initialize, they flash on and go out in unison. If they don't come on, or come on and stay on, the board is most definitely broken. In normal operation, after all the lights have gone out, the controlling application that runs the board can program the lights on each LS-22-SE board to have a unique pattern. This is often beneficial. The nature of PCI is such that if multiple instances of the same board are plugged into the same bus, there will be no visible way to tell one board from another. Finally, the channel 0's FPGA uniquely has eight bidirectional lines (open drains with pull-ups) that go to an "XD" molex

connector, designated J5, whose pads are along the top board edge. They connect to an I/O port for factory test purposes.

2.5 PCI Interface

The PCI interface for the LS-22-SE is a PLX Technologies PCI9080. The PCI interface is set up to map, aside from the 9080's own registers, 64 bytes of PCI I/O space. No memory space is mapped. While there are memories on board, each is mapped to one two-byte area in I/O space. This I/O space is divided as follows:

0x00….0x0F: Channel-0 I/O Reads/Writes.
0x10….0x1F: Channel-1 I/O Reads/Writes.
0x20….0x2F: Channel-2 I/O Reads/Writes.
0x30….0x3F: Reads from this space return meaningless data. Writes to this space are considered broadcasts and write to like registers in all channels at once.

3 INSTALLATION AND CONIGURATION

Chapter 3 provides installation and configuration information. This chapter will locate serial numbers and product configuration information, familiarize the user with the layout of the board, and provide information on the proper installation and interconnection of the hardware.

3.1 Product Outline Diagrams

Figure 3-1 on page 16 and Figure 3-2 on page 17 contain photographs of the top and bottom sides of the LS-22-SE Spectral & Oscilloscope Display Card. Connector locations and switch positions are indicated. The model number, serial number, revision information and product options are denoted as shown right and as indicated in Figure 3-1.

3.2 Addressing

The LS-22-SE Spectral & Oscilloscope Display Card is designed around the Peripheral Component Interconnect (PCI) specification. PCI is an interconnection system between a microprocessor and attached devices in which expansion slots are spaced closely for high-speed operation. Using PCI, a computer can support both new PCI cards while continuing to support Industry Standard Architecture (ISA) expansion cards, an older standard. One characteristic of the PCI architecture is that the cards do not have fixed address assignments, and as such, the LS-22-SE card has no address switches or jumpers to set.

3.3 Physical Installation

To install the LS-22-SE in the target computer system, the following procedure should be followed:

1. Perform a normal system shutdown of the PC system and remove the primary power plug.

Warning:
Installation of display card in a powered platform will cause immediate damage to the interface hardware. Ensure that power is removed from the system prior to hardware installation.

2. Install the LS-22-SE in an unobstructed PC slot ensuring that the card is properly seated in the interface bus socket. PCs vary in their mechanical configurations so it may be necessary to remove additional PC hardware to properly install the LS-22-SE.

3. Install a screw in the mounting panel to secure the unit. Some platforms also have a vertical hold down which can be adjusted to provide additional mechanical stability.

3.4 Indicators

The LS-22-SE has four chip LED indicators shown right that are located along the top edge of the card (see Figure 3-2 on page 17). These LEDs are board identification indicators that are connected to a static register and are intended for use by device drivers in environments where multiple cards are present to identify each of the cards. Additionally, there are three LED indicators on the PCI panel (see Figure 3-3 on page 18). These have meaning only when the optional LS-40-DB Bit Synchronizer Daughterboard is installed. From left to right, these indicators are defined as bit synchronizer signal present, bit synchronizer lock, and bit synchronizer signal quality. Refer to the LS-40 PCM Bit Synchronizer Technical Manual for interpreting these indicators (Doc. No. U4000201).

3.5 Shunt Patches

As shown in Figure 3-1 on page 16, located near the lower left-hand corner of the card are four, 3-pin patch arrays. Each patch array allows for a 2mm shunt patch. For orientation purposes, glance at the back-side of the card and make note of the location of pin 1 for each patch. Pin 1 is indicated by means of a *square* pad. The four patch arrays are designated; E5, E4, E13, and E9 and perform the following function:

- E5: Shunt Pins 1 and 2 to terminate the auxiliary bit synchronizer input with 75 ohms to ground. When this option is used, the termination jumper JP2 on the LS-40 module must be removed. To use the LS-40 JP2 termination option instead, shunt pins 2 and 3 on E5.

- E4: Shunt Pins 1 and 2 to terminate the Baseband In-1 with 75 ohms to ground. Pin 3 is for factory use.

- E13: Shunt Pins 1 and 2 to terminate the Baseband In-2 with 75 ohms to ground. Pin 3 is for factory use.

- E9: Shunt Pins 1 and 2 to terminate the Baseband In-3 with 75 ohms to ground. Pin 3 is for factory use.

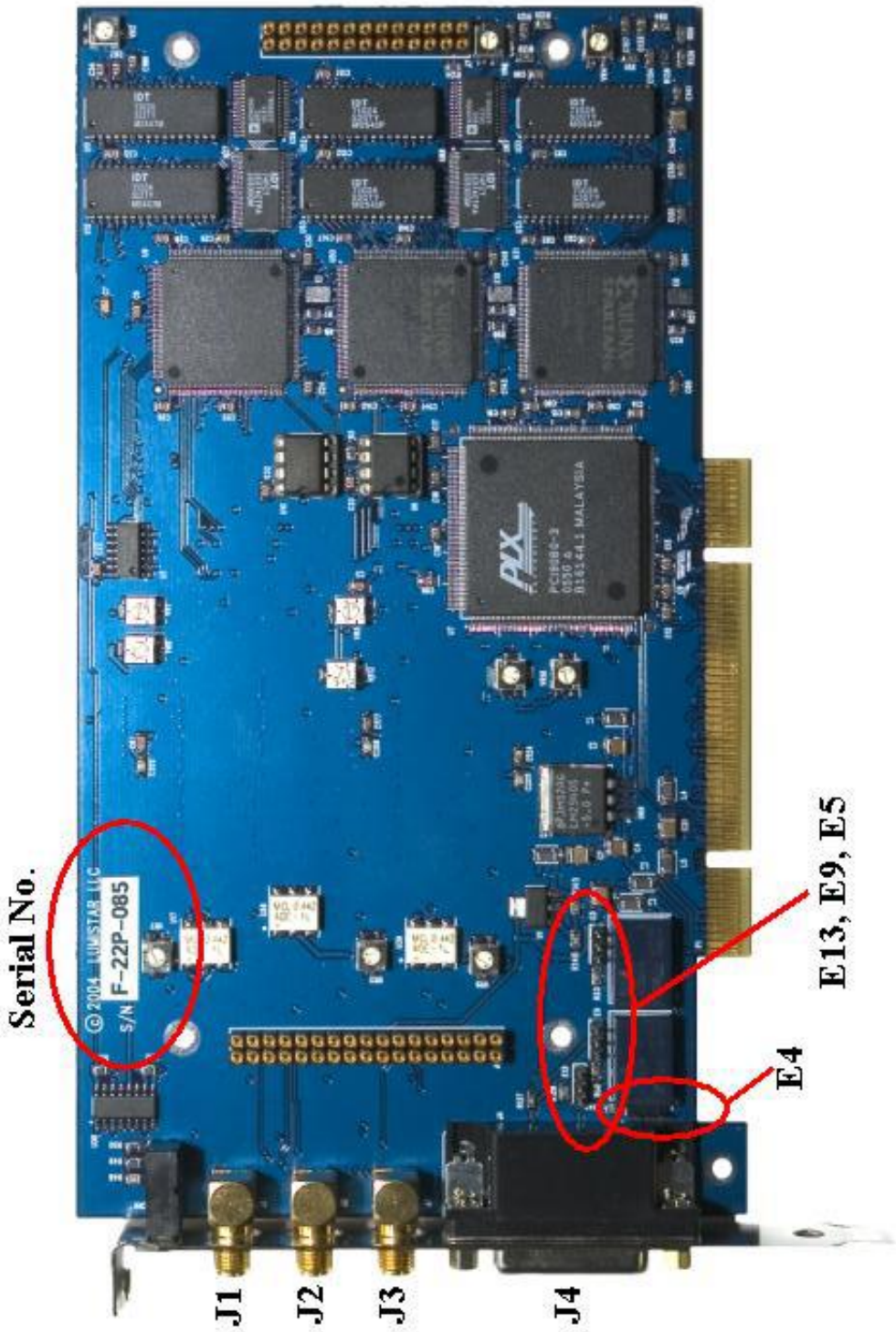


Figure 3-1 LS-22-SE PCI Card (Component Side)

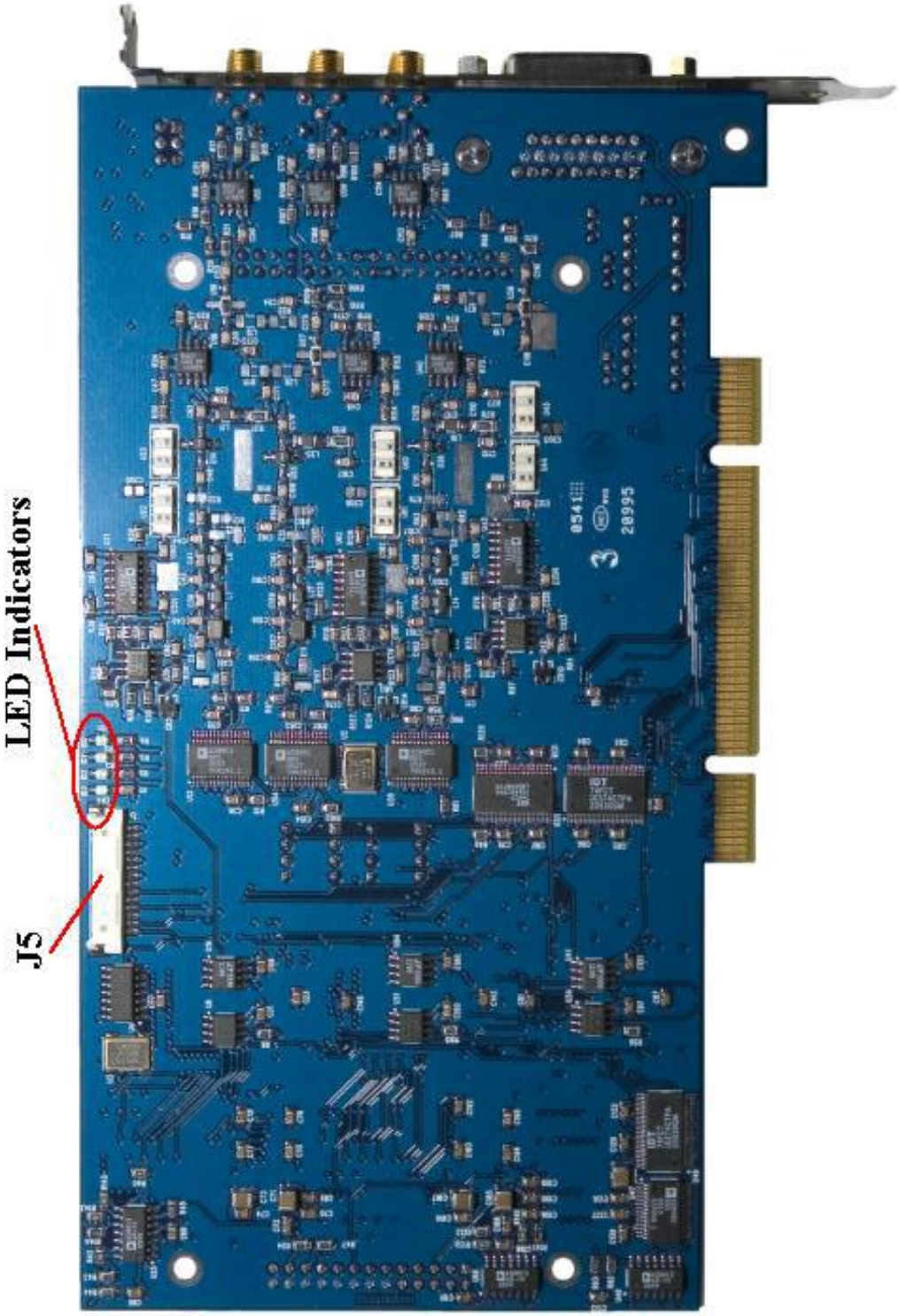


Figure 3-2 LS-22-SE PCI Card (Solder Side)

3.6 Interfaces

The LS-22-SE Spectral & Oscilloscope Display Card is configured at the factory with one, two, or three input channels (see Figure 3-3 below). Both a 70 MHz IF and baseband I/O are provided for each of the configured channels. These interfaces are described in the following paragraphs.

3.6.1 70 MHz IF Inputs

Each of the configured channels has a 70MHz IF input that employs an SMA Connector. As shown in Figure 3-3 below, from the top down these inputs are designated J1, J2, and J3 and are the IF inputs for spectral display channels 1 through 3 respectively. The nominal input signal level is –20dBm.

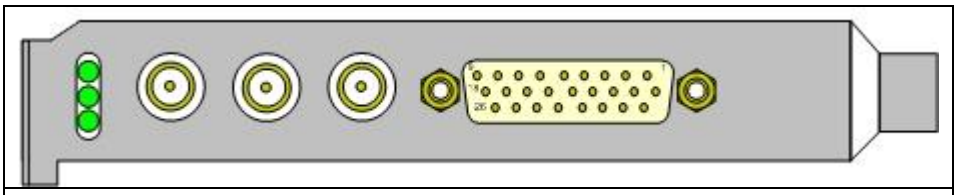


Figure 3-3 PCI Panel Diagram

3.6.2 Baseband I/O Inputs

The subminiature 26-pin connector designated J4 shown in Figure 3-3 above provides the baseband I/O for the LS-22-SE. The pin outs for the J4 connector are shown in Table 3-1 on page 18.

The Baseband In signal (1, 2, and 3) is the input for the oscilloscope displays. Any of these baseband inputs may also be selected as an input for the optional daughterboard bit synchronizer module. The signal level at each input is fixed at approximately 4 Volts p-p for full-scale oscilloscope deflection.

The Status line (1, 2, and 3) is a TTL-compatible status signal. This pin is connected to an open-drain output driver with weak pull-up, and may thus also be used as a status output.

The Aux Status/Trigger input (1, 2, and 3) is a TTL-compatible signal that may be sensed by any software application, or used as an external trigger input for the oscilloscope display.

The Aux Bit Sync Input may be selected as a separate bit synchronizer input that is not associated with any of the baseband inputs.

The Bit Sync NRZ-L and Clock signals are TTL-compatible outputs. The Bit Sync Tape and Test outputs are bipolar signals, intended for compatibility with instrumentation recorders. When enabled via software on the optional daughterboard Bit Synchronizer, the Test output is a 2^{15}-1 bit pseudo-random test pattern at the bit synchronizer programmed bit rate.

Table 3-1 J4 I/O Connector Pin-out

Pin	Signal	Pin	Signal	Pin	Signal
1	Baseband In 1	10	Ground	19	Aux Bit Sync Input
2	Aux Status/Trigger 1	11	Ground	20	Status 1
3	Not Used	12	Ground	21	Bit Sync NRZ-L Out
4	Baseband In 2	13	Ground	22	Bit Sync Clock Out
5	Aux Status/Trigger 2	14	Ground	23	Status 2
6	Not Used	15	Ground	24	Bit Sync Tape Out
7	Baseband In 3	16	Ground	25	Bit Sync Test Out
8	Aux Status/Trigger 3	17	Ground	26	Status 3
9	Not Used	18	Ground	–	–

3.7 Special I/O

The 14-pin Molex 53780-series connector designated J5 shown in Figure 3-2 on page 17 is located along the top board edge. This is connected to a pseudo-bidirectional I/O port associated with channel 1. The signals here are open drains with weak pull-ups. The connector pin-out is shown in Table 3-2. At present there is no defined usage for this firmware definable input/output.

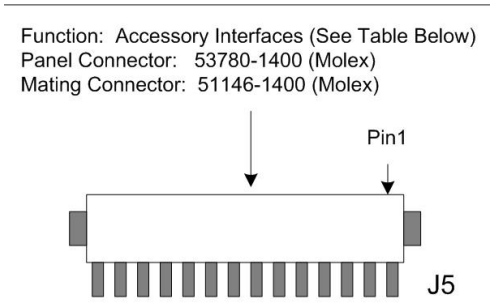


Table 3-2 J5 Special I/O Pin-out

Pin	Signal	Pin	Signal
1	Bit 0	8	Ground
2	Ground	9	Bit 4
3	Bit 1	10	Ground
4	Ground	11	Bit 5
5	Bit 2	12	Ground
6	Ground	13	Bit 6
7	Bit 3	14	Bit 7

3.8 LS-22V3 Interface Cable Assembly

The LS-22-SE Spectral & Oscilloscope Display PCI Card is supplied with a supplementary interface cable assembly shown in Figure 3-4 below. The 26-pin connector is designed to interface with the J4 connector shown in Figure 3-1 on page 16. The specific connector pins of

J4 that are used, the signal names, signal types and connector types are documented in Table 3-3 below. The complete pin-out for J4 is shown in Table 3-1 on page 18.

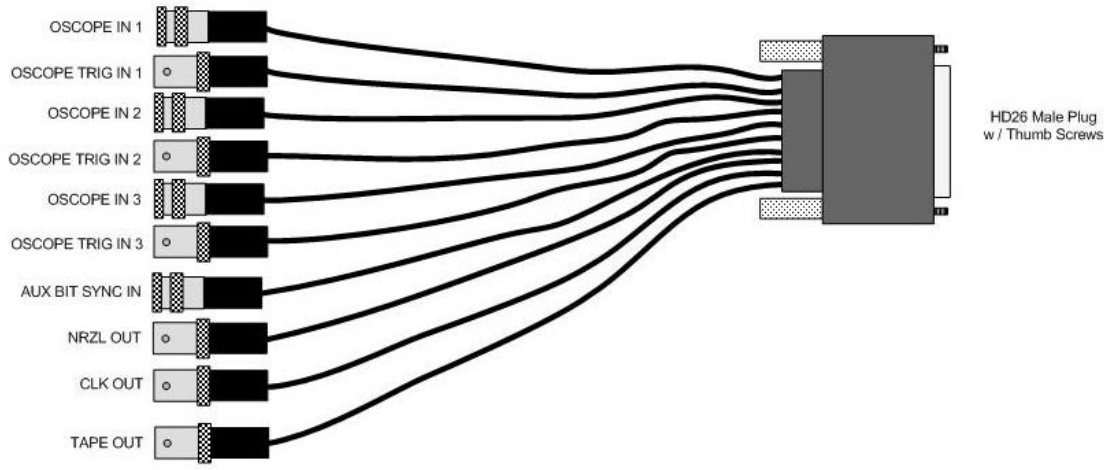


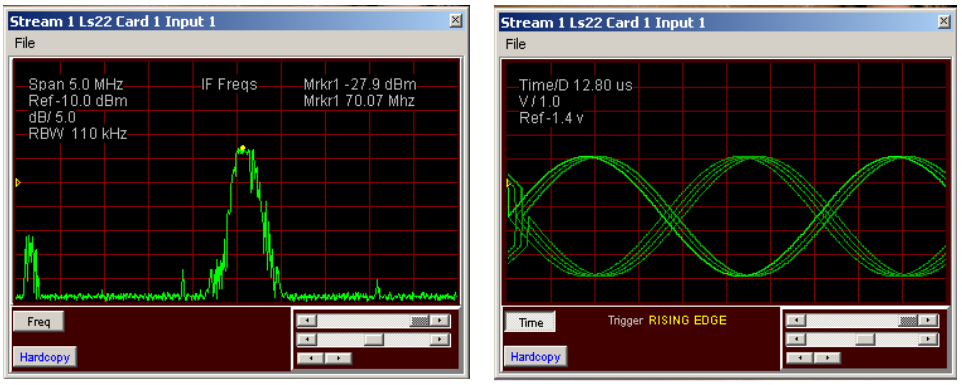
Figure 3-4 LS-22V3 Interface Cable Assembly

Table 3-3 LS-22V3 Interface Cable Assembly Pin Outs

D-Style Connector Pin/ Contact No.	Label Text/Color	Pigtail Type	Signal Details
1	OSCOPE IN1	BNC-M	+/- 4V Input Range
2	OSCOPE TRIG IN1	BNC-F	TTL Input
4	OSCOPE IN2	BNC-M	+/-4V Input Range
5	OSCOPE TRIG IN2	BNC-F	TTL Input
7	OSCOPE IN3	BNC-M	+/-4V Input Range
8	OSCOPE TRIG IN3	BNC-F	TTL Input
19	BIT SYNC IN	BNC-M	LS-40 PCM Input Levels
21	NRZL OUT	BNC-F	RS-422/TTL Output
22	CLK OUT	BNC-F	RS-422/TTL Output
24	TAPE OUT	BNC-F	RS-422/TTL Output
10-18	*(N/A)*	*(N/A)*	Ground

4 Operation of The LS-22-SE With The LDPS Software

The LS-22-SE is a single/multi-channel instrument that supports the display of spectral and time domain information using the Lumistar Data Processing System (LDPS) software (shown below).



Spectral Display ***Time Domain Display (eye pattern)***

Figure 4-1 LDPS Displays for the LS-22-SE

The LDPS is composed of two major application programs - the Server and the Client. The Server program is used to acquire data from various sources (such as the LS-22-SE). The server formats the data into a normalized format, archives it, and then pass the data on to the client application for further processing and/or display. The Client is mainly a data processing and presentation program, with hooks to allow new display and processing routines to be added by the user. The server and client applications can run together on the same computing platform, or on different platforms interconnected via a Local Area Network (LAN). This user's manual will focus primarily on the server side application.

To initially configure the LS-22-SE, perform the following steps:

1. Run the LDPS server program and from the System menu shown below, select "Devices" and then "Manage" *(System→ Devices→ Manage)*
2. From the System Manager shown below left, select the "Enable" check box. The "Ls22Vx_8x" button will then become active (not grayed out). Note the red rectangle around the button - this indicates that the application has not yet started. Note also the "Sim" check box next to the "Enable" check box. Checking this box allows the LDPS application to operate when a LS-22-SE board is not installed in the system.
3. From the System Manager, click the "Ls22Vx_8x" button. This will launch the "Ls22Vx_8x (Scope/Spectrum)" display shown below right.
4. For the spectrum and time-domain displays, follow the procedures outlined in paragraphs 4.1 and 4.2.

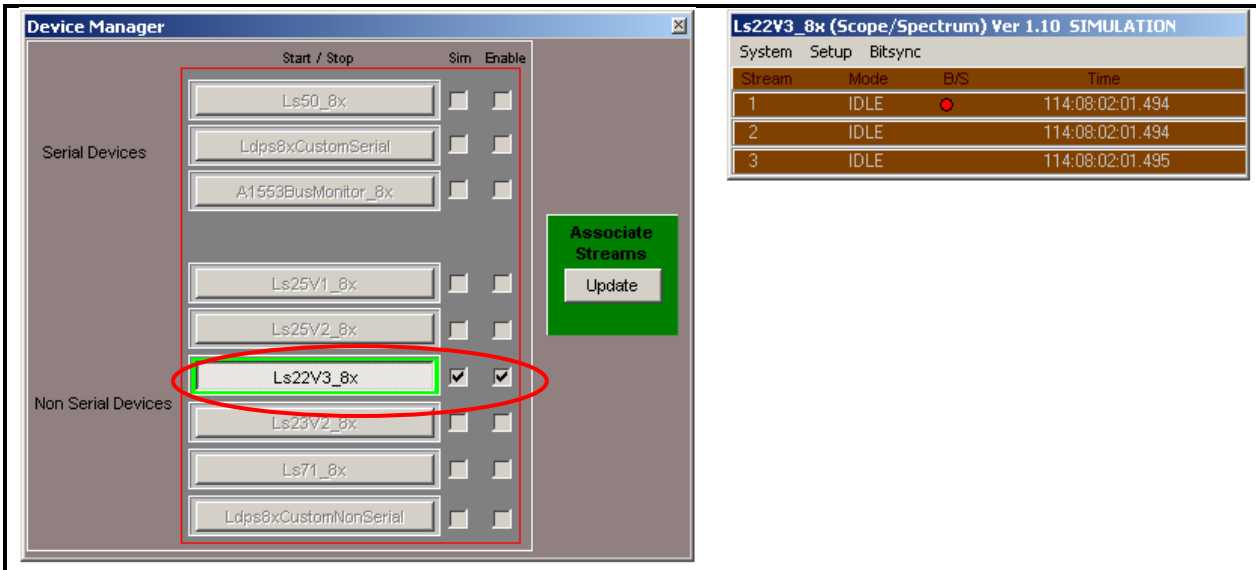


Figure 4-2 LDPS Server Application Windows

4.1 The Spectral Display

From the "Ls22Vx_8x (Scope/Spectrum)" display shown right in Figure 4-2 on page 22, click "Setup" and then "Card Input 1" *(Setup →Card Input 1).* The LS-22-SE Time Domain window shown in the upper left of Figure 4-10 on page 31 will be launched. Click on the "Time" button of the Time Domain display to toggle into the Spectral Display mode. The resulting window is shown in Figure 4-3 below upper left. Also notice that the "Mode" of Card Input 1 has changed from "IDLE" to "SPECTRUM" as shown in Figure 4-3 below lower right. The other inputs of the LS-22-SE card are configured in a similar manner *(Setup →Card Input 2, 3, etc).*

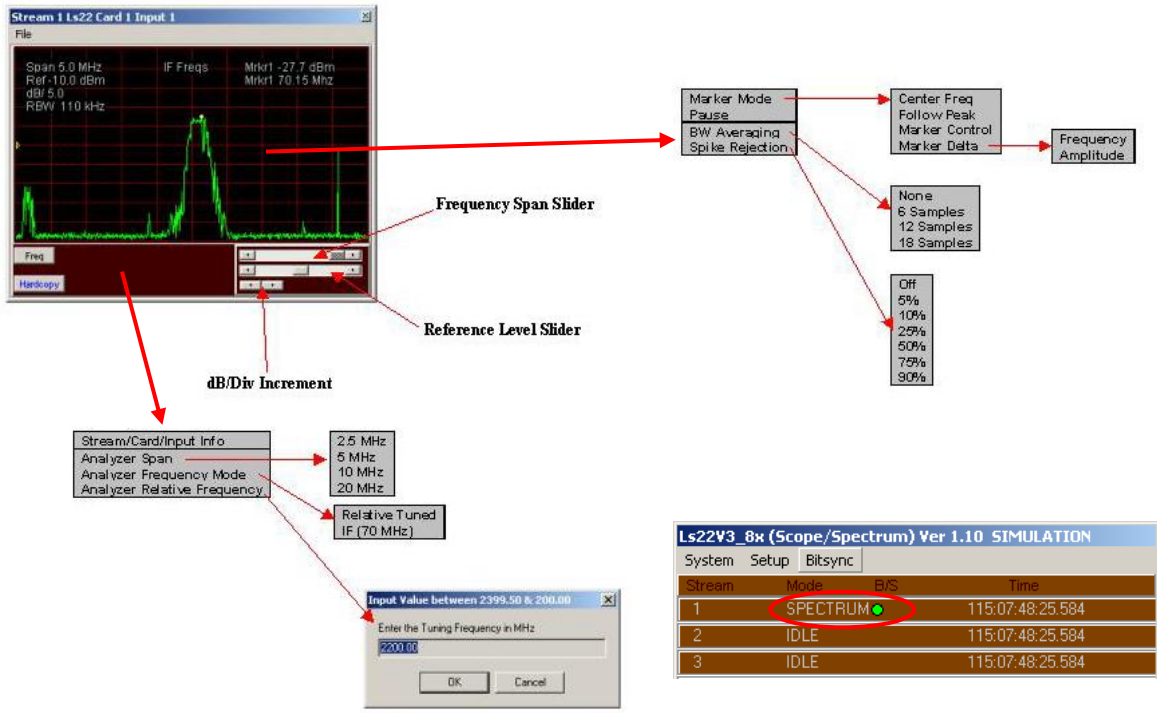


Figure 4-3 LDPS Spectral Display Menus/Controls

The "Ls22Vx_8x (Scope/Spectrum)" display shown in Figure 4-4 below is divided into several regions. In the upper portion of the window is the graphical data display area where the spectrum graphs are generated. Also in the upper left portion of the spectrum display as shown in the red rectangle are the frequency span, the reference level (dB), dB/division, and the resolution bandwidth. These parameters are controlled in the lower right region below the graphical display has slider or knob controls as shown in the figure. Addition information associated with frequency and amplitude markers are shown in the upper right portion of the spectrum display.

To invoke the controls for either the upper or lower portions of the display, simply place the mouse curser in the region and right click. The resulting menus are shown in Figure 4-3 above and are discussed in detail in the following paragraphs.

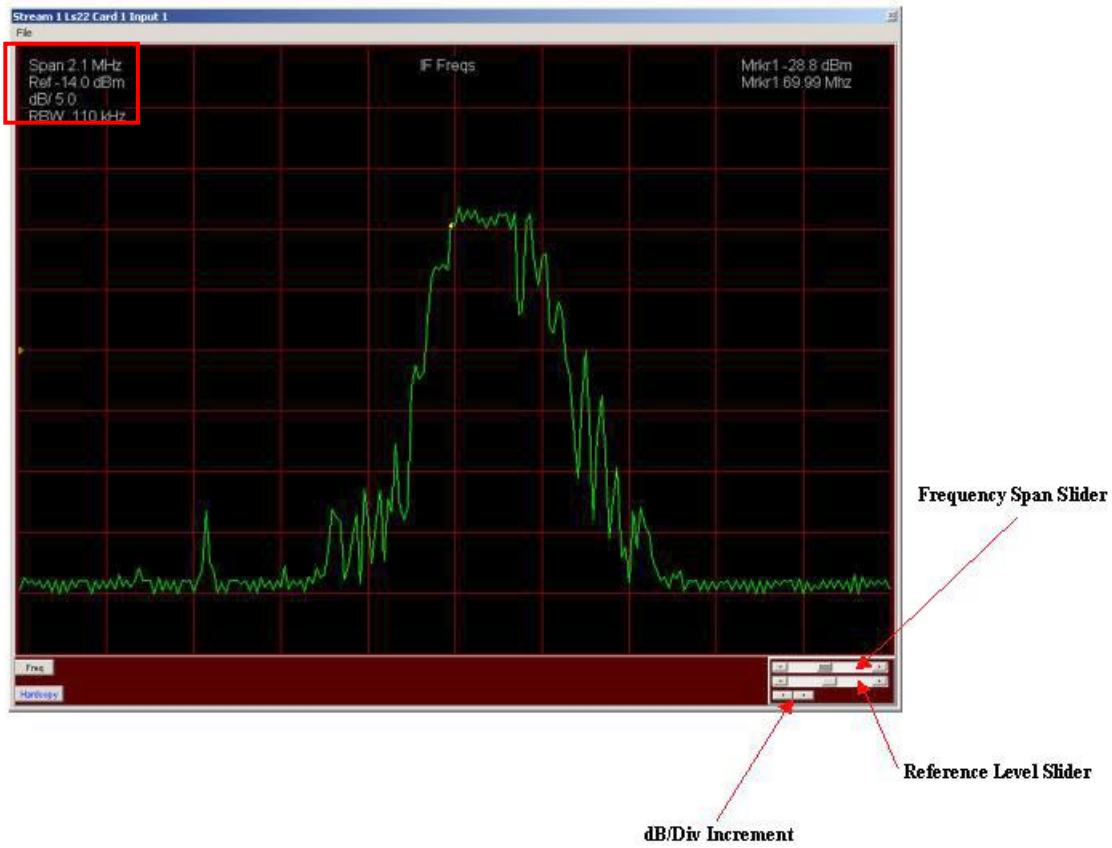
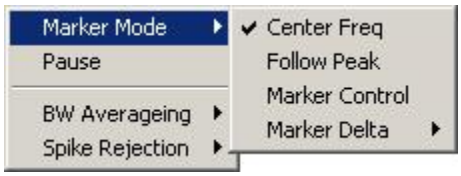


Figure 4-4 The Spectrum Display

4.1.1 Marker Mode

Select the Marker Mode by right clicking in the upper portion of the spectrum display. The Marker Mode has four sub-modes: Center Frequency, Follow Peak, Marker Control, and Marker Delta. Each in turn is discussed in the following paragraphs.



4.1.1.1 Center Frequency

The Center Frequency marker mode places the marker (shown in the red circle in the figure below) at the center of the span of frequencies shown in the display. Note also that the markers amplitude and frequency are shown on the display as indicated in the red square in the figure below.

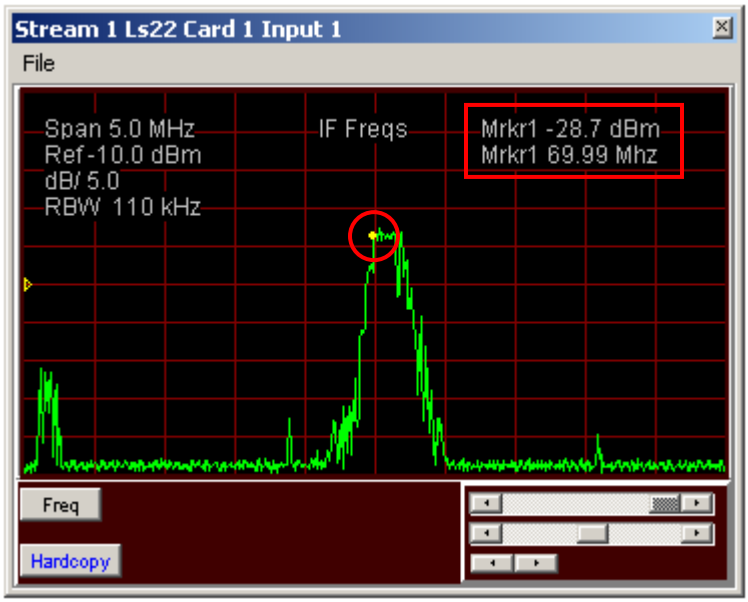


Figure 4-5 Marker Mode → Center Frequency

4.1.1.2 Follow Peak

The Follow Peak marker mode places the marker (shown in the red circle in the figure below) at the peak amplitude value of the trace shown in the display. As the peak value changes in both amplitude and frequency, the marker will move up and down, left and right to follow. Also note as before that the markers amplitude and frequency are shown on the display as indicated in the red square in the figure below.

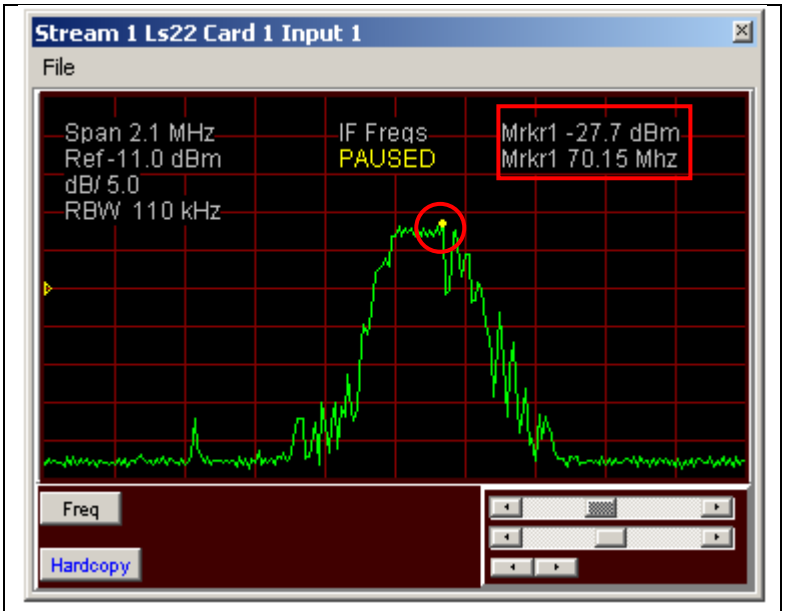


Figure 4-6 Marker Mode → Follow Peak

4.1.1.3 Marker Control

The Marker Control mode places the marker (shown in the red circle in the figure below) at a specific frequency point value on the trace shown in the display. As the amplitude value at that frequency changes, the marker will move up and down. Also note the location of the frequency control shown on the display as indicated in the red square in the figure below. The frequency of the marker is advanced by clicking on the right pointing arrow. Clicking on the left pointing arrow decrease the frequency of the marker.

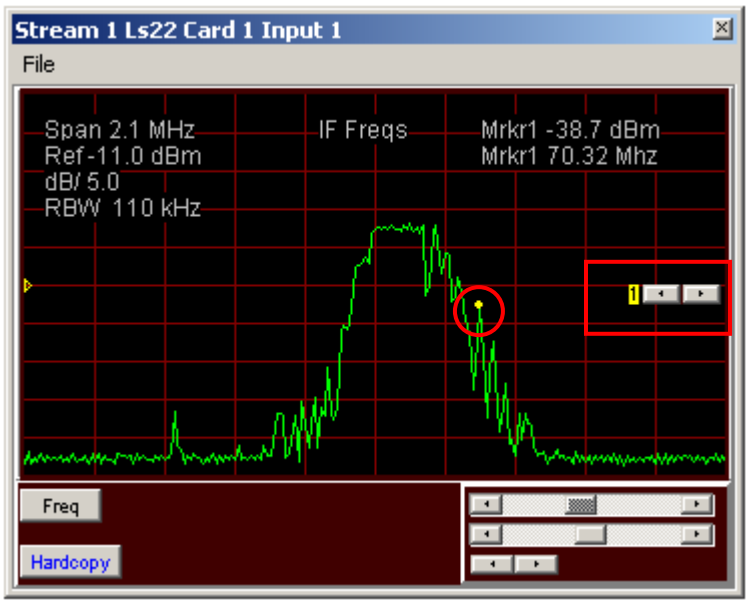
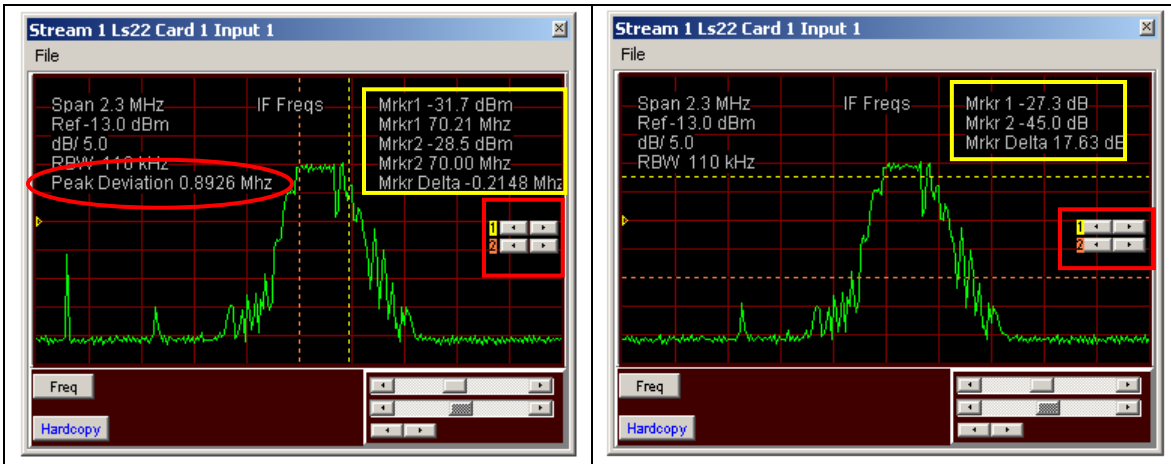


Figure 4-7 Marker Mode → Marker Control

4.1.1.4 Marker Delta

The Marker Delta mode has two sub-modes - Frequency and Amplitude. The Frequency Marker Delta mode is shown left in Figure 4-8 below and is represented by two vertical dotted lines. Each marker line advances or recedes in frequency via the control shown on the display as indicated in the red square in the figure below. Note that the markers amplitude, frequency, and frequency delta are shown on the display as indicated in the yellow square in the figure below. Also note the "Peak Deviation" parameter shown in the red oval on the left side of the spectral display. This parameter only has meaning when the spectrum of a NRZ/FM signal is being displayed, and is meaningless otherwise.



Delta Frequency Markers	***Delta Amplitude Markers***

Figure 4-8 Marker Mode → Marker Delta

The Amplitude Marker Delta mode is shown right in Figure 4-8 above and is represented by two horizontal dotted lines. Each marker line increases or decreases in amplitude via the control shown on the display as indicated in the red square in the figure above. Also note that the markers amplitude, and amplitude delta are shown on the display as indicated in the yellow square in the figure above.

4.1.2 Pause Mode

Select the Pause Mode by right clicking in the upper portion of the spectrum display. This will freeze the updating of the spectrum display and is indicated as shown in the red oval in Figure 4-9 below. To resume the dynamic updating of the spectrum display, again select the Pause Mode by right clicking in the upper portion of the spectrum display. The activation of this mode is indicated by a check mark symbol (√) next to the "PAUSE" item in the menu.

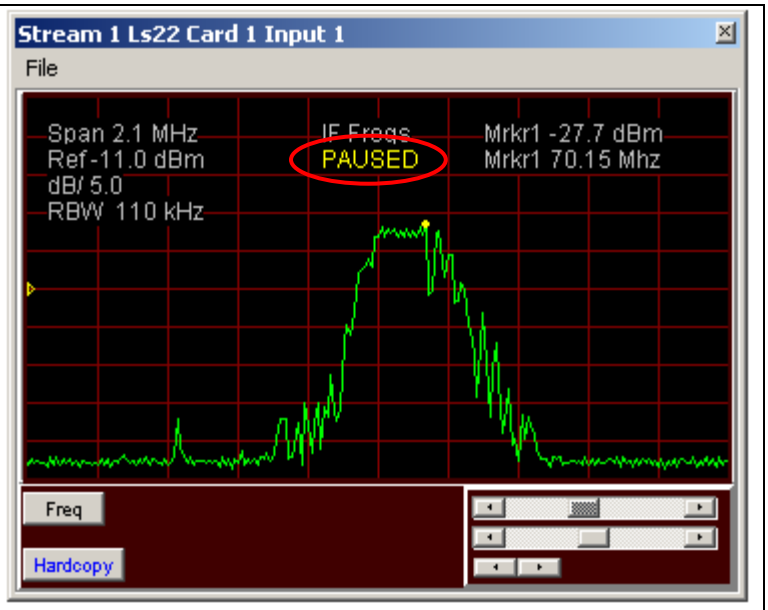
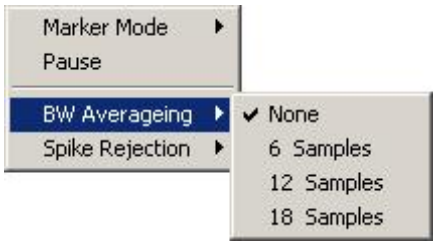


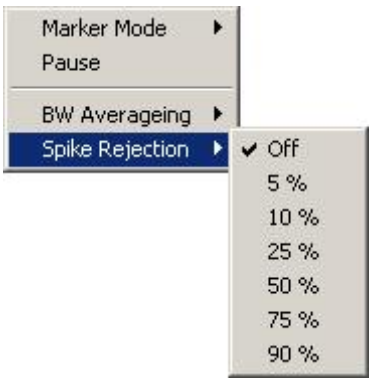
Figure 4-9 Spectrum Display in Pause Mode

4.1.3 Bandwidth (BW) Averaging



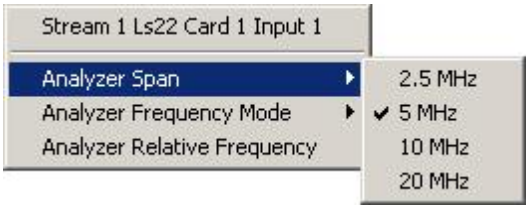
Select the Bandwidth Averaging Mode by right clicking in the upper portion of the spectrum display. The default mode is set to None, but may be set to 6, 12, and 18 samples. When the Bandwidth Averaging mode is selected, the specified number of samples are accumulated and averaged for each point on the display. Thus, each point on the display is updated every 6, 12, or 18 samples, and the value for each point is the average over the 6, 12, or 18 samples. Use the BW Averaging mode to eliminate any random "spikes" that may be seen in the display.

4.1.4 Spike Rejection

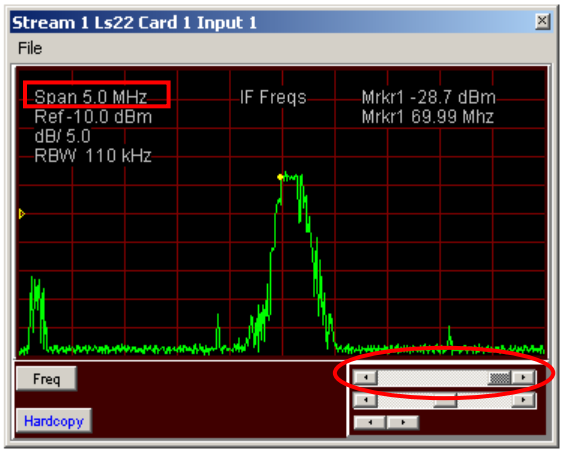


Select the Spike Rejection Mode by right clicking in the upper portion of the spectrum display. The default mode is set to None, but may be set to 5, 10, 25, 50, 75, or 90 percent. The Spike Rejection mode runs each point in the display through a filter that continuously calculates a running standard deviation for each point. For each new point, if the value for the point is outside one standard deviation by the selected value (5, 10, 25, 50, 75, or 90 percent), then that point is thrown away and not displayed. The Spike Rejection mode is more sophisticated than BW averaging, in that it gives the user more fidelity in selecting the elimination of any random "spikes" that may be seen in the display.

4.1.5 Analyzer Span

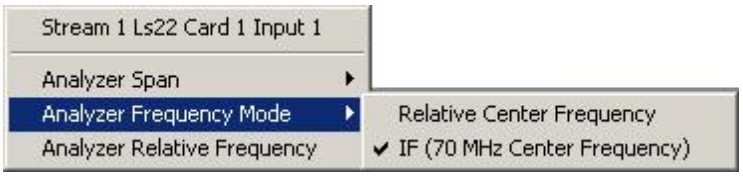


Select the Analyzer Span by right clicking in the lower portion of the spectrum display. The user may select four different frequency display spans that include: 2.5 MHz, 5 MHz, 10 MHz, and 20 MHz. The frequency span value selected is displayed in the upper left portion of the spectrum display as indicated by the red rectangle in the figure below. Frequency spans other than the standard values mentioned in this paragraph may be selected by the user via the frequency span slider shown in the red oval in the figure below.



4.1.6 Analyzer Frequency Mode

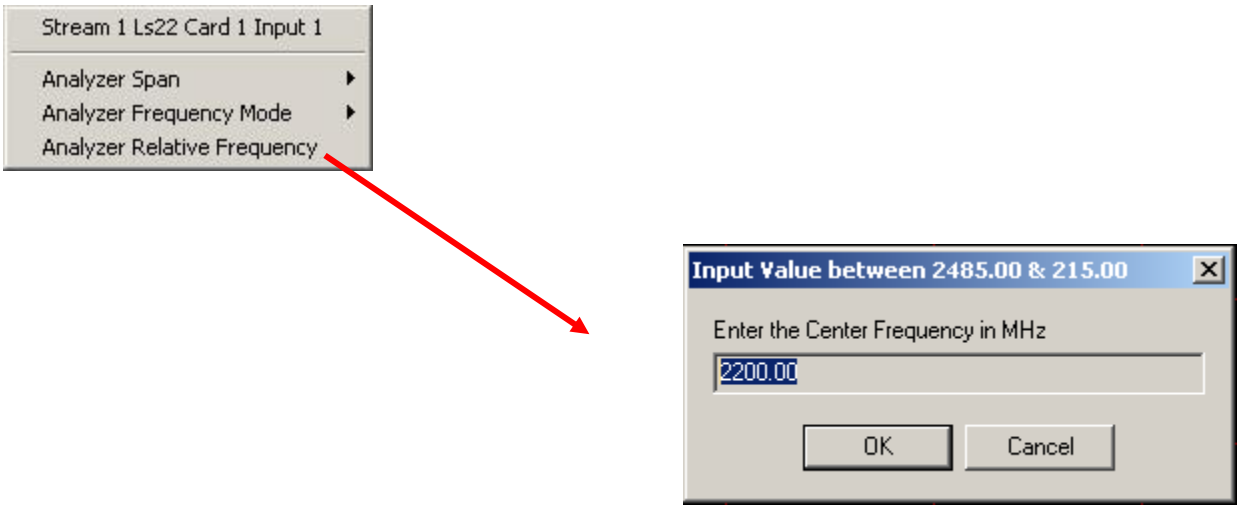
Select the Analyzer Frequency Mode by right clicking in the lower portion of the spectrum display. The user may select Relative Center Frequency, or IF (70 MHz Center Frequency). The default mode is IF (70 MHz Center Frequency). In the IF mode, the center frequency of the display is set to 70 MHz and all measurements are made relative to that. In the Relative Center Frequency mode, the center frequency of the display is set to a value established by the Analyzer Relative Frequency mode (see paragraph 4.1.7 for more info).



4.1.7 Analyzer Relative Frequency

Select the Analyzer Relative Frequency by right clicking in the lower portion of the spectrum display. The value entered in the dialog box may be any frequency between 200 and 2399.5

MHz. In the Relative Frequency mode, the center frequency of the display is set to the entered value and all measurements are made relative to that.



4.2 The Time-Domain Display

From the "Ls22Vx_8x (Scope/Spectrum)" display shown right in Figure 4-2 on page 22, click "Setup" and then "Card Input 1" *(Setup →Card Input 1).* The LS-22-SE Time Domain window shown in the upper left of Figure 4-10 below will be launched. Also notice that the "Mode" of Card Input 1 has changed from "IDLE" to "O'SCOPE" as shown in Figure 4-10 below lower right. The other inputs of the LS-22-SE card are configured in a similar manner *(Setup → Card Input 2, 3, etc).*

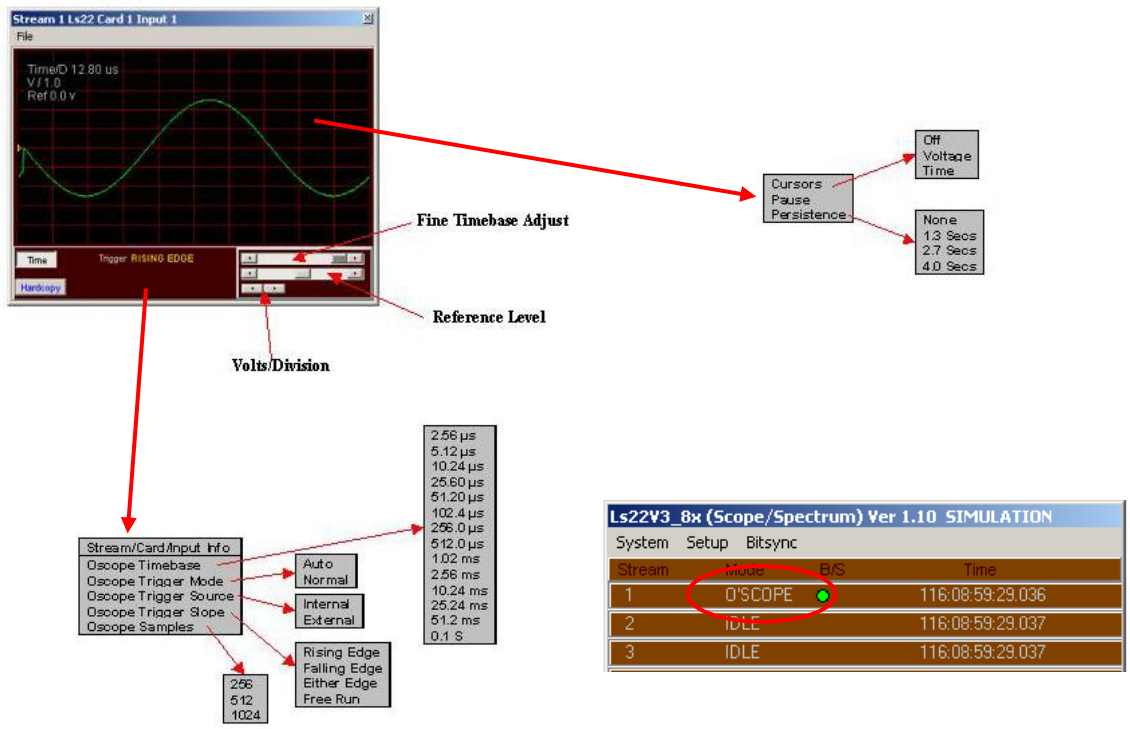


Figure 4-10 LDPS Time Domain Display Menus/Controls

The "Ls22Vx_8x (Scope/Spectrum)" display shown in Figure 4-11 below is divided into several regions. In the upper portion of the window is the graphical data display area where the time domain graphs are generated. Also in the upper left portion of the time-domain display as shown in the red rectangle are the timebase setting, the volts/division, and the reference voltage level. These parameters are controlled in the lower right region below the graphical display has slider or knob controls as shown in the figure.

To invoke the controls for either the upper or lower portions of the display, simply place the mouse curser in the region and right click. The resulting menus are shown in Figure 4-10 above and are discussed in detail in the following paragraphs.

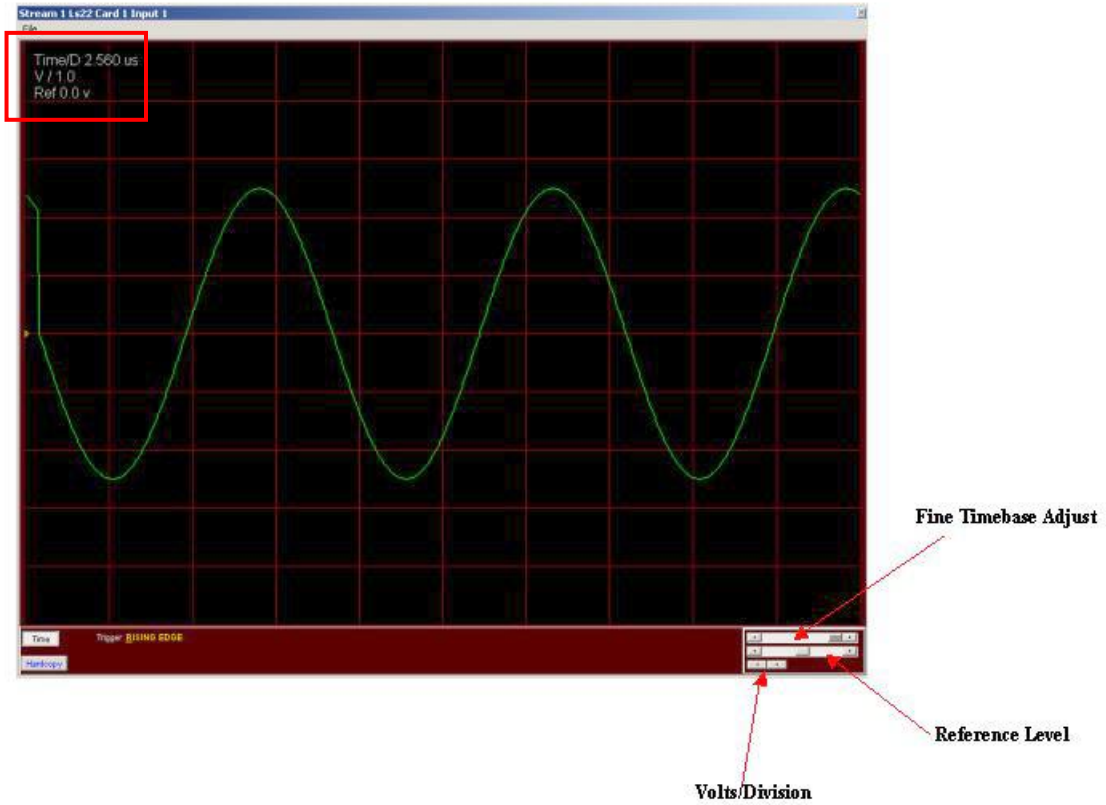
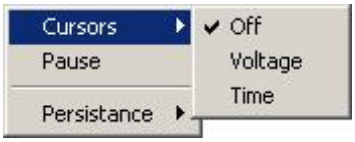


Figure 4-11 The Time-Domain Display (Oscope)

4.2.1 Cursor Controls

Select the Cursor Control Mode by right clicking in the upper portion of the time domain display. The Cursor Control Mode has three sub-modes: Off, Voltage, and Time. Each in turn is discussed in the following paragraphs.



4.2.1.1 Voltage Cursors

The Voltage Cursor mode is shown in Figure 4-12 below and is represented by two horizontal dotted lines. Each marker line increases or decreases in voltage via the control shown on the display as indicated in the red square in the figure below. Also note that the markers voltage, and voltage delta are shown on the display as indicated in the yellow square in the figure below.

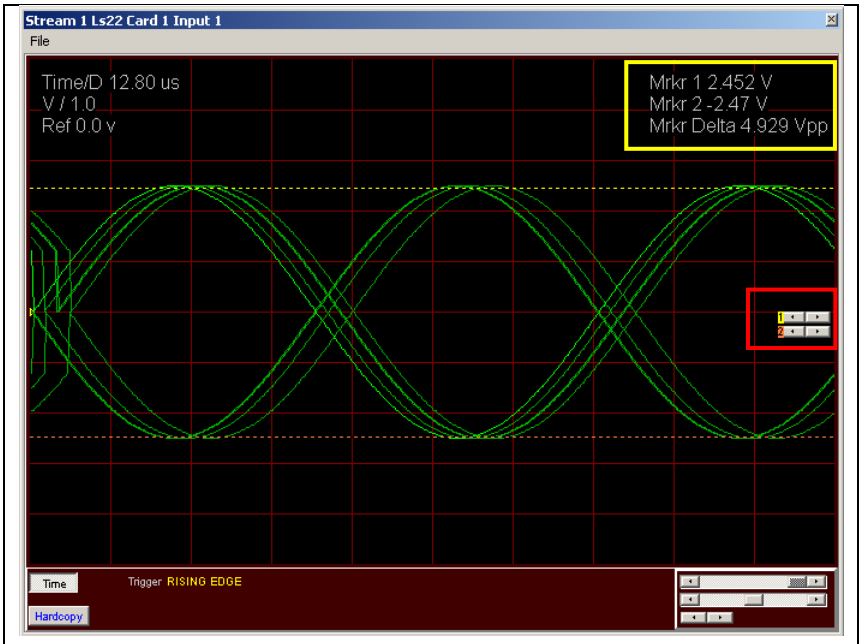


Figure 4-12 Voltage Cursor Mode

4.2.1.2 Time Cursors

The Time Cursor mode is shown in Figure 4-13 below and is represented by two vertical dotted lines. Each marker line advances or recedes in time via the control shown on the display as indicated in the red square in the figure below. Also note that the markers time, and time delta are shown on the display as indicated in the yellow square in the figure below.

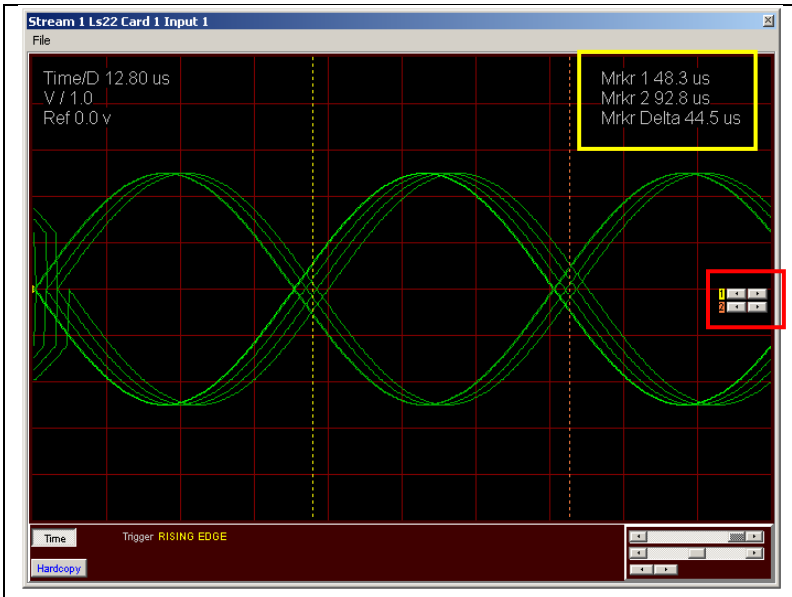
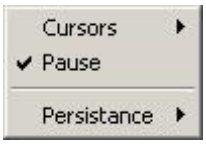


Figure 4-13 Time Cursor Mode

4.2.2 Pause Mode



Select the Pause Mode by right clicking in the upper portion of the time domain display. This will freeze the updating of the time domain display and is indicated as shown in the red oval in Figure 4-14 below. To resume the dynamic updating of the time domain display, again select the Pause Mode by right clicking in the upper portion of the time domain display. The activation of this mode is indicated by a check mark symbol (√) next to the "PAUSE" item in the menu.

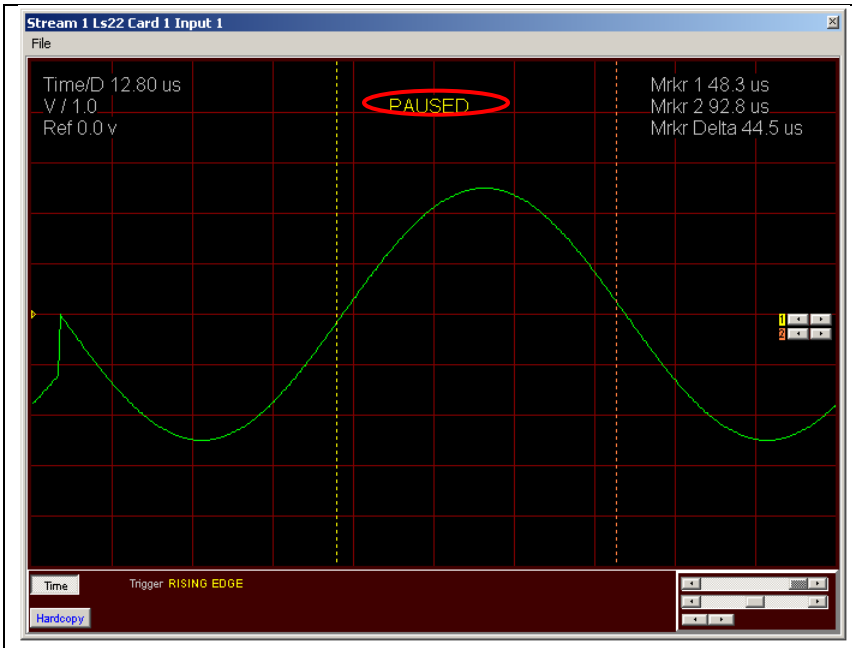
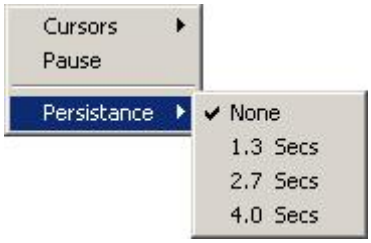
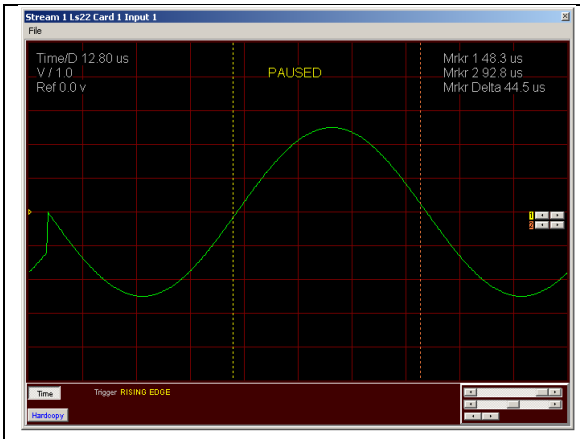


Figure 4-14 Time Domain Display in Pause Mode

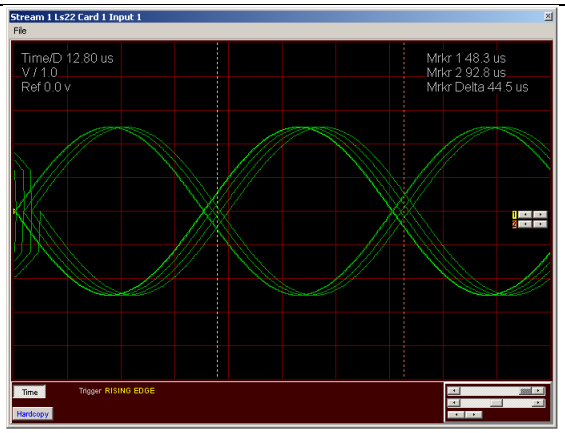
4.2.3 Persistence Control



Select the Persistence Control Mode by right clicking in the upper portion of the time domain display. The Persistence Control has four sub-modes: None, 1.3, 2.7, and 4.0 Seconds. Use the Persistence Control to examine for example the "eye-pattern" of a demodulated datastream. With persistence of the display, successive cycles of a time-varying signal are in essence, displayed one on top of the other, thus creating a temporal layering of successive and often transitory events. An example of this effect is shown right in Figure 4-15 below.



Persistence → None

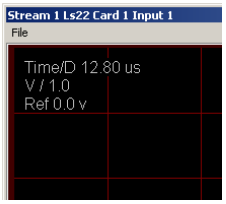


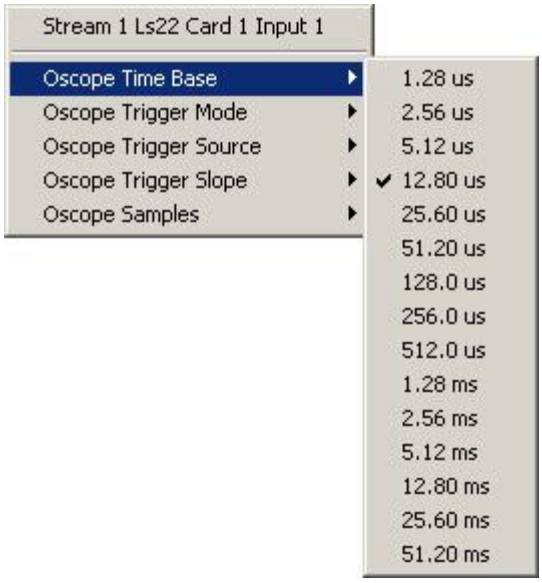
Persistence → 4.0 Seconds

Figure 4-15 Example of Display Persistence

4.2.4 Oscilloscope Timebase Control

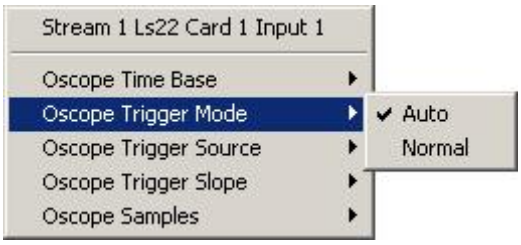
Select the Oscilloscope Timebase Control Mode by right clicking in the lower portion of the time domain display. With the timebase control, the user may select fourteen (14) different display timebase settings. The range of timebase settings depends on the sample size selected from the Oscope Samples Control Mode (see paragraph 4.2.8 for more details), and range from 640 ns to 0.10 s. The Timebase setting (time/division) is display as shown right in the upper left corner of the display area. The range of timebase settings shown below corresponds to a sample size of 512.



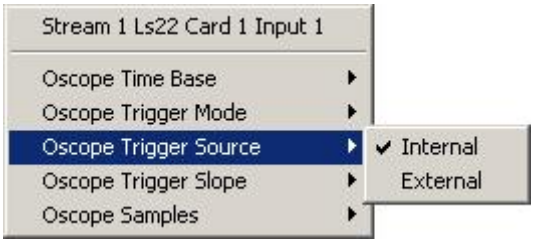


4.2.5 Oscilloscope Trigger Mode

Select the Oscilloscope Trigger Mode by right clicking in the lower portion of the time domain display. The Trigger Mode has two sub-modes: Auto and Normal. In normal mode the oscilloscope only sweeps if the input signal reaches the set trigger condition. Auto mode causes the oscilloscope to sweep, even without a trigger.

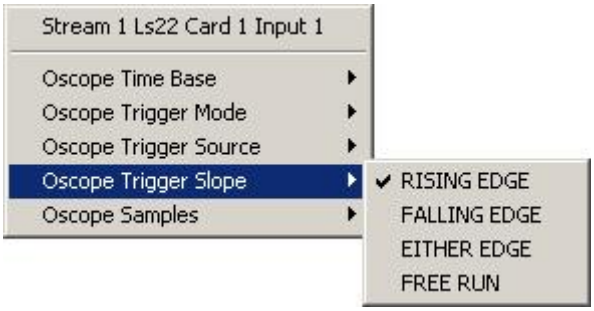


4.2.6 Oscilloscope Trigger Source



Select the Oscilloscope Trigger Source by right clicking in the lower portion of the time domain display. The Trigger Source Mode has two sub-modes: Internal and external. In the Internal mode, the display will be triggered from the signal being displayed. In the External mode, the external trigger signals for each of the three possible channels of the LS-22-SE will be used to trigger the display. See Table 3-3 on page 20 for the pin numbers of the external triggers on connector J4 for more information.

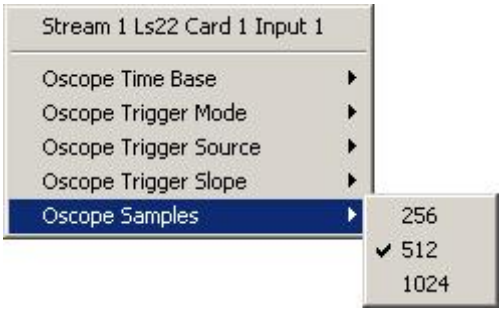
4.2.7 Oscilloscope Trigger Slope



Select the Oscilloscope Trigger Slope by right clicking in the lower portion of the time domain display. The Trigger Slope Mode has four sub-modes: Rising Edge, Falling Edge, Either Edge, or Free Run. In the Rising Edge mode, a positive transition (rising edge) of either the Internal or External trigger will trigger the display. In the Falling Edge mode, a negative transition (falling edge) of either the Internal or External trigger will trigger the display. For the Either Edge mode, both a rising or falling edge of either the Internal or External trigger will trigger the display. In the Fee Run mode, the trigger conditions (rising/falling edges) are ignored and the display continuously updates.

4.2.8 Oscilloscope Samples

Select the Oscilloscope Sample size by right clicking in the lower portion of the time domain display. The Oscilloscope Sample Mode has three sub-modes: 256, 512, and 1024 samples.



4.3 Modifying the Spectral and Time-Domain Controls

Both the Spectral and Time-Domain displays offer several different types of graphical controls. In addition to the standard "slider" controls shown in Figure 4-4 on page 24 and Figure 4-11 on page 32, several additional control configurations are available. To change the type of controls found on the displays, select the server options from the LDPS Server window (System → Options) and click on the "Unique Card Settings" tab. The four different types of controls for the LS-22-SE are shown in Figure 4-16 below. After selecting a particular controls configuration, click the OK button and then from the LDPS Server window restart all devices (System → Devices → Restart). Note: the change in control configuration will only take effect after a reset.

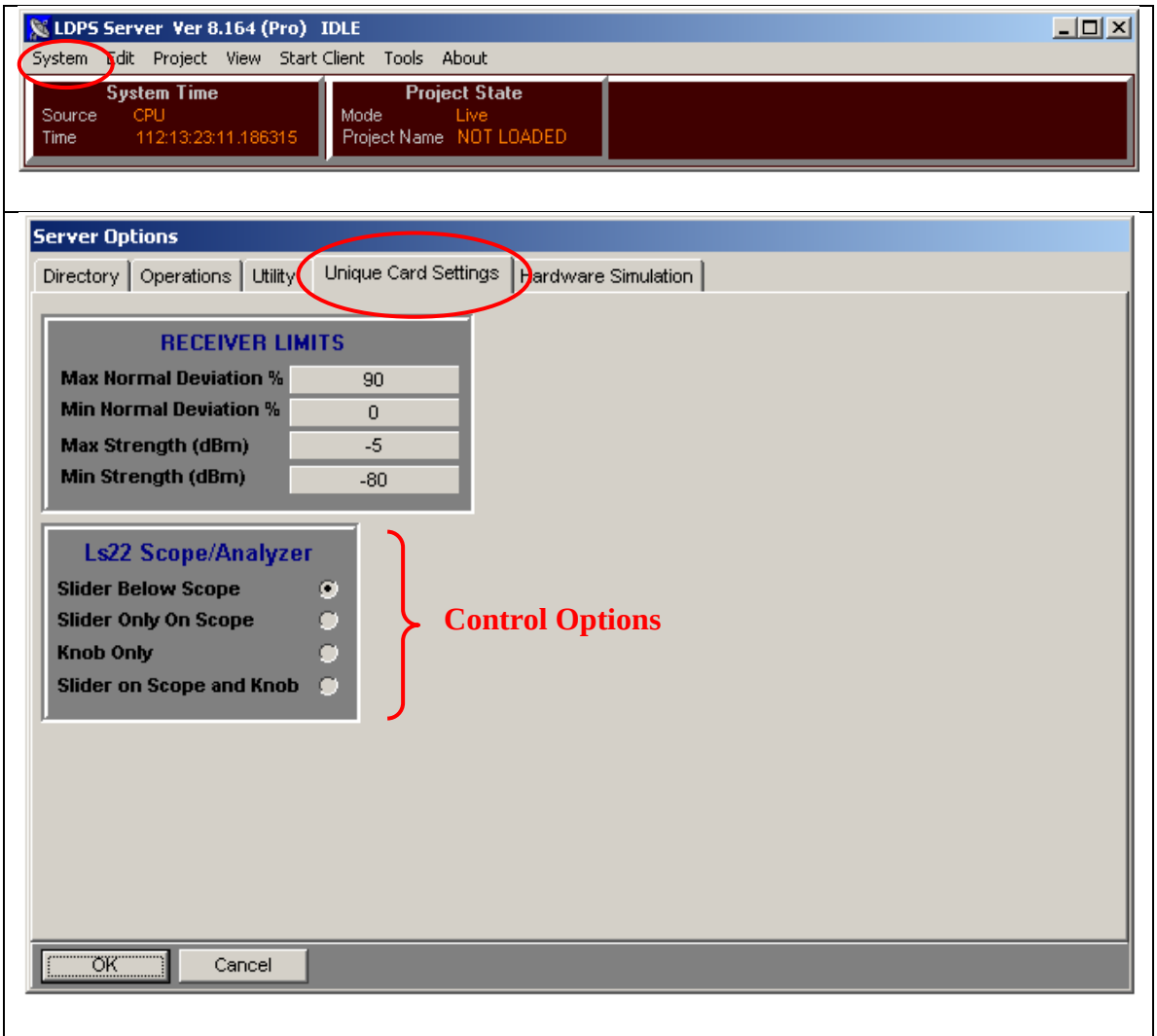
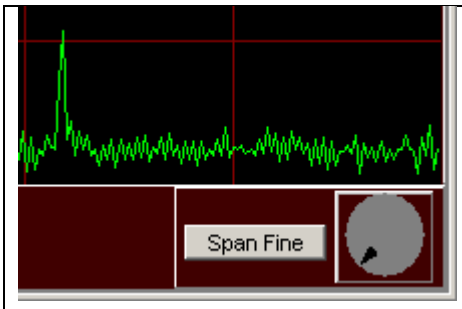


Figure 4-16 LDPS Server Options - Unique Card Settings

The default control configuration, *"Slider Below Scope"* are shown in the various displays seen in the document thus far (Figure 4-4 and Figure 4-11 for example).

In the *"Slider Only On Scope"* configuration, the three sliders at the lower right of the display are moved to locations in the upper portion of the display. For example, the frequency span slider in the spectral display or the fine timebase adjustment slider in the time-domain display appear as a large horizontal scroll bar extending across the entire upper edge of the display. The reference level slider in both the spectral and time-domain displays appear as a large vertical scroll bar extending across the entire left edge of the display. The dB/division for the spectral display and Volts/division for the time-domain sliders appear as single up/down arrows in the upper left portion of the display. To invoke any of these slider controls for this configuration, place the mouse cursor in the upper portion of the display and right click and select the parameter to adjust. Once selected, the slider control will persist until a different slider is selected.

In the *"Knob Only"* configuration, the three horizontal sliders at the lower right of the display are replaced by a single multi-function virtual knob and a parameter selection button. Clicking on the button will cycle through the available adjustment parameters. To make an adjustment, select a parameter and place the mouse cursor on the knob and click and hold the mouse button while rotating the knob with the mouse. For the spectral display, the available adjustment parameters include: Fine Span, Course Span, dB/Division, and Reference Level. For the time-domain display, the available adjustment parameters include: Fine Timebase Adjust, Volts/Division, Vertical Position, and Course Timebase Adjust.

	
Spectral Display	***Time-Domain Display***

The *"Slider On Scope and Knob"* configuration is a simple union of the "Slider Only On Scope" and "Knob Only" configurations described previously.

5 PROGRAMMING

5.1 General

This chapter on programming is intended for software developers who indent to create custom application programs that will make use of the LS-22-SE and its capabilities. These custom applications could run under any operating system that supports the standard Intel/AMD processor architecture implemented in a PCI environment. For those users who require an existing, off-the-shelf application to control the LS-22-SE, The Lumistar Data Processing System (LDPS) software application would be an ideal choice. LDPS is a powerful, client/server data acquisition, processing, and visualization tool that runs under Microsoft Windows XP/2000. Consult the factory for more information on the LDPS software and a copy of the documentation.

The LS-22-SE is controlled by an array of registers. Each register is eight bits long and identified by a register number. The following paragraphs describe these registers in more detail

5.1.1 PCI Systems

As mentioned previously, PCI components like the LS-22-SE do not have fixed address assignments (set with jumpers or switches). Rather, at system startup a power-up routine running in the BIOS scans the computer for PCI interfaces and assigns system resources to those components that are discovered.

On non-PC architectures one may run into *"Big/Little-Indian"* issues that the user should be aware of.

Each PCI component discovered by the BIOS is assigned an array of sixty-four, 32-bit registers in what is referred to as the "configuration space." This area is normally not accessible anywhere in the system address space and must be accessed by special means that are system-dependent.

The following discussion illustrates how to access the configuration space of the LS-22-SE and applies to systems using MS-DOS or Microsoft Windows where the PCI configuration space is accessed via BIOS calls. Other operating system environments will have system-specific ways of accessing this information. To locate the LS-22-SE board in your system, perform the following steps:

1. Initialize an "index" value to zero. The index will be used in a code loop to scan for PCI devices. This index is allowed to be as large as 255 by the PCI specification, but in practice never gets this large.

2. To locate the PCI9080 bus control/interface chip(s) for each PCI device, set the machine registers as follows:

AX = 0xB102
CX = 0x9080
DX = 0x10B5
SI = *index*

3. Issue a software interrupt 0x1A. If the system returns from the interrupt with the carry flag set, then all such devices are already located and no more exist. In this event, skip out of the scanning routine. If the system returns from the interrupt with the carry flag clear, then the BIOS call will have returned a "handle" in the BX register.

4. With the carry flag set to clear, read the sub-identifier and set the registers as follows:
AX = 0xB10A
BX = handle
SI = 0x2C

5. Issue another software interrupt 0x1A. The interrupt will return a value in ECX. If the value returned is 0x0222B00B, then the handle will points to one of the boards. If the returned value in ECX is not 0x0222B00B, then skip to step 7. Set the registers as follows:
AX = 0xB10A
BX = handle
SI = 0x1C

6. Issue another software interrupt 0x1A. Logically AND the value returned in ECX with 0x0FFF0. The result yields the base I/O port. Registers defined below are in the PCI I/O space and map simply according to the following relationship:

$$k = s + ((0x10) \times (c - 1)) + r$$

where "r" is a register, "c" is a LS-22-SE channel number (1,2 or 3), "s" is the base I/O port, and "k" is the I/O address.

7. Increment the index value and scan for more cards.

5.2 I/O Channels

The LS-22-SE is factory configured with either one, two, or three display channels. Each channel has its own associated array of control registers. As shown in the search algorithm in the preceding paragraph, the channel number changes the register address. Reads and writes to an I/O address 0x0n offset from the board address refers to channel-1. Reads and writes to I/O address 0x1n refers to channel-2, and address 0x2n refers to channel-3. Reads from address 0x3n are meaningless, but writes to address 0x3n will write to all channels simultaneously, however many are present. See paragraph 5.3.2 below to detect how many physical channels are installed.

5.3 Programming Details

The control register bit assignments are shown below in Table 5-1 and Table 5-2. In some cases read and write bit assignments for the same register are different. Bits defined by a dash (–) do not physically exist. Bits named ONE and ZERO are intended for factory use. At the application level these bits always need to be as implied.

5.3.1 Initialization

There is no defined startup sequence for the LS-22-SE. After a system restart the initialization process happens automatically. An attempt to read the status register *immediately* after a restart will show the BUSY flag to be set (the initialization after restart takes only a few hundred milliseconds, so it will likely be finished before any code has started running). After a system restart, the ONE bit in the command register comes up set (true).

Table 5-1 Write Register Summary

Register	#	7	6	5	4	3	2	1	0
Not Defined	00	–	–	–	–	–	–	–	–
Board ID*	01	–	–	–	–	ID3	ID2	ID1	ID0
Aux Command	02	GO	–	–	–	–	–	–	CLR
Command	03	GO	Norm	Mode	Stop	SWEEP		ONE	CLR
EEPROM Command	04	WR	RD	Address					
EE Data Lo	05	EEPROM Data LSBs							
EE Data Hi	06	EEPROM Data MSBs							
Not Used	07	–	–	–	–	–	–	–	–
Sample Data Lo	08	Test Data Lsbs							
Sample Data Hi	09	–	–	–	–	–	–	Test Data	
Timebase	0A	SSIZE		–	Scope Sample Rate				
Trigger	0B	–	–	–	–	–	–	EXT	–
Special I/O*	0C	(to be defined)							
(Factory Test)	0D	–	–	–	–	–	–	–	–
Bit Sync Command*	0E	Bit Sync Command Data							
Bit Sync Control*	0F	–	–	–	–	–	!Stb	SOURCE	
* Meaningful only for Channel 1									

5.3.2 Board Identifier

Successive reads from the "Identifier" register eventually return the ASCII string "βLS22SEβ" where β is a null. There is an identifier register for each channel. Only channels physically installed will return an identifier (they all return the same string.) By convention, channel 1 is always installed. If channel 2 is present, channel 3 may be present. If channel 2 is absent, channel 3 is also absent.

5.3.3 Board ID Register

The Board ID register controls a set of indicators along the top edge of the board (see Figure 3-1 on page 16). The device driver or application should set this register uniquely. This will resolve any ambiguity about the identity of each board. The four high-order bits of the ID register are reserved for future use. When setting a board ID, these bits should be set to zero for forward compatibility. Reading the register will return the value written.

Table 5-2 Read Register Summary

Register	#	7	6	5	4	3	2	1	0
Identifier	00	0	(Identifier String)						
Board ID*	01	–	–	–	–	ID3	ID2	ID1	ID0
Not Defined	02	–	–	–	–	–	–	–	–
Status	03	Busy	–	Mode	Stop	SWEEP		Pin4	Done
Not Defined	04	–	–	–	–	–	–	–	–
Not Defined	05	–	–	–	–	–	–	–	–
EE Data Lo	06	EEPROM Data LSBs							
EE Data Hi	07	EEPROM Data MSBs							
Sample Data Lo	08	Sample Data LSBs							
Sample Data Hi	09	0	0	0	0	0	0	Sample Data	
Not Defined	0A	–	–	–	–	–	–	–	–
Not Defined	0B	–	–	–	–	–	–	–	–
Special I/O*	0C	(to be defined)							
Not Defined	0D	–	–	–	–	–	–	–	–
Bit Sync Read back*	0E	Bit Sync Read back Data							
Bit Sync Status*	0F	1	Read	!SQ	!Pres	1	Busy	Lock	Sig
* Meaningful only for Channel 1									

5.3.4 EEPROM Access

64 sixteen-bit words of configuration EEPROM are installed. Clamp the address in the range [0..0x3F], add 0x40 and write to the EEPROM Command register. BUSY will be set for about 15 microseconds. When it clears, one can safely read the EE Data registers.

5.3.5 Command Register

The command register is primarily used to control the sampling functions of the LS-22-SE. The register is read/write but the read definitions of some bits are only related to their write definitions, as noted in the Table 5-3 below. Only one type of sample can be taken at a time, but the user may change the MODE bit whenever BUSY is not set and alternate samples in succession.

5.3.6 Auxiliary Command Register

The GO and CLR bits from the command register reappear here.

Table 5-3 Command Register

Bit	Definition
0 (R)	DONE. Set by an end-of-sample event triggered by writing to the GO bit.
0 (W)	CLR. Writing a one clears the bit and clears the memory address counter. Writing a zero has no effect.
1	PIN4/ONE. State of the rear-plate external status input. If the status line is unused, returns value written. If the status line is used as an input, this bit should always be written as a one.
2..3	SWEEP. This field changes meaning based on the MODE bit setting. If MODE = 0 the field selects the scope trigger slope. If MODE = 1 the field specifies the width of the spectrum span. Read returns the value written. Value MODE = 0 MODE = 1 0 Rising Edge 5MHz 1 Falling Edge 10MHz 2 Either Edge 20MHz 3 Free Run 40MHz
4	STOP. Disables acquisition. For test purposes only. Read returns the value written.
5	MODE. Selects Sample type. Zero selects a scope sample. One selects a spectrum display sample. Do not change this bit while BUSY is set. Also controls the polarity of data read from acquisition memory. Read returns the value written.
6 (R)	STAT. Returns state of Status/Trigger input.
6 (W)	NORM. Scope trigger mode. A zero-crossing is normally required to trigger the scope If NORM = 1 the scope will wait forever if necessary. If NORM = 0 the scope will free-run if it has waited 4096 sample periods without seeing a trigger condition. If the EXT bit is set in the Trigger register the Aux Status input is a TTL-Compatible external trigger. Otherwise the scope trigger is by a zero-crossing at the baseband input.
7 (R)	BUSY. Returns busy status. One indicates an EEPROM access or a data sample is in progress.
7 (W)	GO. Writing a one initiates a sample (selected by MODE.) Writing zero has no effect.

5.3.7 Timebase Register

The timebase register sets operating parameters for the oscilloscope display option. Fields are defined in Table 5-4 below.

Table 5-4 Timebase Register

				Sample Size	
VALUE	**Sample Rate**	**Value**	**Sample Rate**	**SSIZE**	**Size**
0x01	40MHz	0x0B	100kHz	0	256 Points
0x02	20MHz	0x0D	40kHz	1	512 Points
0x03	10MHz	0x0E	20kHz	2	1024 Points
0x05	4MHz	0x0F	10kHz		
0x06	2MHz	0x11	4kHz		
0x07	1MHz	0x12	2kHz		
0x09	400kHz	0x13	1kHz		
0x0A	200kHz	0X00	Stopped		

5.3.8 Acquisition Memory

When the LS-22-SE samples data, the instrument gathers either baseband signal level or spectral data for each of the configured channels as selected by the MODE bit and stores it in on-board memory. The memory access is sequential and works like a FIFO. Sample Data (see Table 5-2, registers #08, & #09) is retrieved from this register and occupies the ten LSBs of memory, the MSBs always read zero. You can safely read (or write) the Sample Data register memory when BUSY is not set.

Don't try to mix reads and writes. This will yield gibberish.

The first read of the Sample Data (after issuing a CLR command) returns the value of the first location. The subsequent read of the register returns the next location, and so on. A sample always fills in points starting at the first location. The number of scope samples is determined by SSIZE (see Table 5-1, register #0A). Spectral samples are always 512 points. Note that scope data in the real memory is inverted. The MODE bit controls the sense of the memory contents to correct this, so when reading sample data out, keep the MODE bit unchanged from when the sample was taken. Sixteen-bit I/O accesses to the memory are permitted. Eight-bit accesses may also be used if the low-order byte is read first.

5.3.9 Bit Synchronizer Daughterboard

The LS-22-SE provides connectors to host a Lumistar LS-40-DB10 or LS-40-DB20 Bit Synchronizer Daughterboard. The bit synchronizer may be connected to any of the three baseband inputs, or to an uncommitted auxiliary input. See Table 5-5 below for more information. If the bit synchronizer is properly set up to accept the incoming data stream, the serial data and reconstructed clock will be available at the rear plate (see Table 3-1 on page 18 and Figure 3-3 on page18).

If a Bit Synchronizer Daughterboard is installed, the "!PRES" bit of the Bit Sync Status register will be set to zero (see Table 5-2, register #0F). Control of the bit synchronizer is through the address space of Channel-1, regardless of the actual input selected. The LS-40 module is configured by writing a sequence of command bytes to the Bit Sync Command register. See the LS-40 Series User's Manual (Doc. No. U4000201) for more details. After writing to the Command register, write a zero, and then a one to the "!STB" bit in the Bit Sync Control register. This toggle causes the command byte to be written to the LS-40 and the BUSY bit to come on briefly.

Certain commands cause the LS-40 to return status messages as a string of bytes. When the LS-40 receives one of these, it will reassert the BUSY bit, format up the status message, and set the READ bit in the Bit Sync status register. This reverses the direction of the Bit Sync Data register. When READ is set and BUSY is clear, a byte of the status message can be read back from the data register. Accept the character by writing zero, then one to the !STB bit. This sets Bit Sync BUSY, which persists until the next character may be read. After you have accepted the last character the LS-40 will clear the READ bit.

Table 5-5 Bit synchronizer Source

Source	Selection
0	Channel 1
1	Auxiliary Input
2	Channel 2
3	Channel 3