Description:

The Lumistar LS-50-D PCI Multi-function PCM Decommutator offers a PCM decom, PCM simulator, time code reader/generator, and optional bit synchronizer in a single short PCI card slot. The multi-function decom and simulator are implemented in FPGA using a next generation design based on the LS-50-P. The simulator, decommutator, time code reader and time code generator are achieved on the main board and the bit synchronizer is achieved through an optional low-profile daughterboard. CVSD voice decoding, h.261 video decoding, and IRIG Chapter 8 decoding are achieved through software.

The IRIG Time Code Reader and Generator operate with IRIG A, B, or G time codes. The Time Code Reader is typically used to insert time information into the PCM minor frame block of data. The Time Code Generator creates and outputs time information in accordance with the IRIG Time Code Standards. Both reader and generator are capable of operating at ½, 1, and 2 times the normal rate.

The Decom can be used for extremely large formats (65,536 words per minor frame up to 1,024 frames deep) and contains dual ping-pong data output buffers with up to 128K bytes of memory.

The PCM simulator generates common, unique, and waveform pattern data words or pseudo-random test pattern (11 through 25 bit) to allow bit error loop calculations to be performed. Five-pole Butterworth pre-modulation filtering is provided with 16 selectable data rates from 100 Kbps to 20 Mbps which complies with the IRIG telemetry filtering requirements.

Key Features:

- PCI Multifunction PCM Decommutator containing
  - PCM Simulator with pre-mod filtering and BERT generating capability
  - PCM Simulator or BERT generating modes
  - PCM Decommutator with BERT reading capability
  - IRIG Time Code Reader and IRIG Time Code Generator
- LS-40/45-DB Bit Synchronizer Daughterboard - Optional (10, 20 or 25 Mbps)
- CVSD Voice, h.261 Video and IRIG Chapter 8 Decoding through LDPS-Pro Software
- Short PCI Board only 7.5 inches long
SPECIFICATIONS:

PCM DECOMMUTATOR:

- **Input Data Rate**: 64 bps to 20 Mbps
- **Input Signals**: NRZ-L data & 0 degree clock
- **Input Levels**: Single-ended TTL & RS-422
- **Word Length (VWL)**: Variable from 3 to 16 bits per word on a word-by-word basis
- **CRC checker**: CRC16/CCITT
- **Minor Frame Length**: 2 to 65,536 words per minor frame
- **Major Frame Length**: Up to 1024 minor frames per major frame
- **Bit Order**: MSB or LSB-first (word-by-word basis)
- **Frame Sync Pattern**: Up to 64 bits (any pattern with don’t care bits (X) may be used)
- **Frame Sync Location**: Beginning or end of the frame
- **Frame Sync Strategy**: Adaptive mode (search-lock-verify) & burst mode (search-lock)
- **Sync Error Tolerance**: 0 to 15 bits (selectable)
- **Sync Slip Window**: 1, 3, 5, or 7 bits wide (selectable)
- **Data Polarity**: Normal, inverted or automatic
- **Subframe Sync**: FCC (FAC), SFID or URC (Optional)
- **URC Location**: Any 64 bit window within the first minor frame not including the last bit in the minor frame
- **SFID Location**: Any series of contiguous bits not including the last bit in the minor frame

IRIG A/B/G READER/GENERATOR:

- **Time Reader Input Format**: IRIG A, B, or G
- **Time Reader Rate**: ½, 1, or 2 times normal rate
- **Input signal level**: 1V p-p nominal
- **Latency**: 2μsec (maximum)
- **Data Outputs**: Automatic time tags for PCM data blocks (time accessible in register space)
- **Time Generator Output**: IRIG A, B, or G
- **Time Generator Rate**: ½, 1, or 2 times normal rate

MECHANICAL:

- **PCI**: PCI Board 7.55” Long
- **Daughterboard Form Factor**: LS-40/45-DB for Bit Synchronizer

POWER REQUIREMENTS:

- **5V**: 850 ma
- **-12 V**: 120 ma
- **+12V**: 30 ma

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